IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
SHERMAN DIVISION

STMICROELECTRONICS, INC.,	§	
	§	
Plaintiff,	§	Civil Action No. 4:03-CV-276 (LED)
	§	
v.	§	
	§	
MOTOROLA, INC.,	§	
	§	
Defendant,	§	
Counterclaim Plaintiff,	§	
	§	
v.	§	
	§	
STMICROELECTRONICS, N.V., and	§	
STMICROELECTRONICS, INC.,	§	
	§	
Counterclaim	§	
Defendants	§	

MOTOROLA'S MOTION TO ENFORCE PARAGRAPH 3–7 OF THE COURT'S PATENT RULES

More than one month after the deadline for disclosing asserted claims—and only one week before the parties must exchange a list of claim terms to be construed—STM submitted a new list of asserted claims and new charts setting forth its allegations of infringement.[1] The new list and charts were submitted without leave of Court and without establishing good cause as required by Patent Rule 3-7. And, despite Motorola's requests, STM failed to identify any basis

[1] STM provided its P.R. 3–1 disclosure of asserted claims to Motorola on October 31, 2003, asserting one claim from U.S. Patent No. 5,812,789 ("the '789 patent") and one claim from U.S. Patent No. 5,031,092 ("the '092 patent," collectively "the STM patents"). STM also accused Motorola of infringing four claims from U.S. Patent No. 5,359,244, but has not attempted to supplement its contentions with respect to this patent; for purposes of this motion, all references to "the STM patents" refer only to the '092 and '789 patents. *See* Disclosure of Asserted Claims and Preliminary Infringement Contentions of Plaintiff STMicroelectronics, Inc. ("Disclosure of Asserted Claims"), attached hereto as Exhibit A ("Ex. A").

26

for its untimely identification of the 26 new claims.[2] Indeed, STM cannot justify its untimely assertion of the new claims since, with the exception of one newly-identified product, the claims are being asserted against the exact ***same products*** relying on the exact ***same documents*** that were in STM's possession prior to its October 31st Disclosure of Asserted Claims.[3]

Accordingly, Motorola asks the Court to enforce P.R. 3–7 by striking STM's First Supplement to Disclosure of Asserted Claims and Preliminary Infringement Contentions and requiring STM to seek leave to amend and show good cause for doing so before permitting the untimely addition of new claims.

I. STATEMENT OF FACTS

On October 31, 2003, STM served its P.R. 3–1 Disclosure of Asserted Claims and Preliminary Infringement Contentions on Motorola, alleging that several Motorola products infringed "at least" claim 23 from the '092 patent, claim 1 from the '789 patent and claims 1, 13, 14 and 15 of the '244 patent.[4] Motorola notified STM on November 19 that the Patent Rules required them to disclose all claims that the identified products allegedly infringe by October 31, and that STM would be precluded from identifying additional claims without good cause.[5] STM disagreed, and did not identify any additional claims with respect to the accused products.[6]

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[2] Letter from Hilda Galvan to Bruce Sostek dated December 5, 2003 (Ex. H).

[3] STM has for the first time accused the i.MX Applications Processor with Hantro's Multimedia Framework of infringing claims 5, 6, 7, 8, 13, 15, 16, 17, 18, 19, 20, 21, 22, 23, and 28 of the '789 patent. Because STM has failed to identify the basis for the supplementation, it is unclear ***when*** the information relied on by STM for its infringement allegations was in its possession Thus, with respect to this product and the claims asserted against this product, Motorola requests that the Court order STM to comply with P.R. 3-7 and that, until such time, the Court strike claims 5, 6, 7, 8, 13, 15, 16, 17, 18, 19, 20, 21, 22, 23, and 28 from STM's Disclosure of Infringement Contentions and Preliminary Infringement Contentions.

[4] Disclosure of Asserted Claims (Ex. A).

[5] Letter from Hilda Galvan to Bruce Sostek dated November 19, 2003 (Ex. B).

[6] Letter from Bruce Sostek to Hilda Galvan dated November 21, 2003 (Ex. C).

On November 24, Motorola again notified STM that P.R. 3–1 required STM to have disclosed all asserted claims because (1) by December 11 the parties must identify all claim terms that must be construed by the Court and (2) Motorola's invalidity contentions and corresponding document production are based on the claims identified in STM's P.R. 3–1 disclosure.[7] STM again disagreed, arguing that the patent rules should not "be applied in a purely rigid and mechanistic fashion" and that "flexibility" was required.[8] Once again, STM did not identify any additional claims with respect to the accused products.[9]

On December 1, Motorola served its P.R. 3–3 Preliminary Invalidity Contentions and P.R. 3–4 Document Production Accompanying Preliminary Invalidity Contentions based on the claims identified by STM in its P.R. 3–1 disclosure.[10] Several days later, STM hand-delivered a new set of disclosures to Motorola identifying 26 new claims from the two of the three STM patents.[11] STM's original and supplemental contentions with respect to these two STM patents are summarized below:

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[7] Letter from Hilda Galvan to Bruce Sostek dated November 24, 2003 (Ex. D).

[8] Letter from Bruce Sostek to Hilda Galvan dated November 26, 2003 (Ex. E).

[9] *Id.*

[10] Preliminary Invalidity Contentions (excerpts of which are attached as Ex. F).

[11] First Supplement to Disclosure of Asserted Claims and Preliminary Infringement Contentions of Plaintiff STMicroelectronics, Inc. (Ex. G). In its First Supplement, STM also accuses an additional Motorola product of infringing the '789 patent.

U.S. Patent No. 5,812,789		
Accused Products	**Original Identified Claims**	**New Identified Claims**
MCT4000 MCT4100 MCT5100 RD2 Reference Design Platform	1	2, 3, 4, 14
i.MX Applications Processor with Hantro's Multimedia Framework	none	5, 6, 7, 8, 13, 15, 16, 17, 18, 19, 20, 21, 22, 23, and 28
U.S. Patent No. 5,031,092		
Accused Products	**Original Identified Claims**	**New Identified Claims**
DSP56305 DSP56F801/803/805/807 DSP56321 DSP56362 MC68332 MC68336 and MC68376 MPC555 and MPC556 MPC565 and MPC566 MPC7410 MPC7441/7445 MPC7450/7451/7455	23	6, 10, 11, 12, 23, 24, and 25

Except for one newly-identified product (i.MX Applications Processor), STM accused the ***exact same*** products relying on the ***exact same*** documents in its new contentions as it did in its original contentions.[12]

The December 1 disclosure of claims and contentions was served without leave of Court in contravention of P.R. 3–7, and despite Motorola's request, STM failed to identify any good faith basis for adding the new claims.[13]

II. STM SHOULD BE REQUIRED TO COMPLY WITH PATENT RULE 3-7

The Patent Rules and the Courts' Proposed Dates for Docket Control Order and Discovery Order ("the Court's schedule"), as agreed to by both parties, provide a fair and orderly

[12] Exs. A, G.

schedule for disclosures in order to pave the way for a timely claim construction and to avoid gratuitous tactical gamesmanship. Under the Court's schedule and P.R. 3–1, the parties were to identify all asserted claims by October 31, 2003. This provides the parties with 42 days to analyze the asserted claims before claim terms must be identified for construction under P.R. 4-1.[14] As provided by P.R. 3–7, a party may amend or modify its P.R. 3–1 disclosures only by order of the Court, which shall be entered only upon a showing of good cause.

Notwithstanding these rules and deadlines, more than one month after Motorola was to be put on notice of all of STM's asserted claims—and only one week before claim term disclosures were due—STM served an additional, untimely set of disclosures, without leave of Court, changing its contentions with respect to the two STM patents from two claims to 28 claims. Moreover, except for one newly-accused product, STM relied on the exact same documents in every one of its new claim charts as it did in its original P.R. 3–1 disclosures. Indeed, many of the newly-added charts contain claim element descriptions that were merely copied—word for word—from STM's original charts.[15] There was no newly-identified or previously-unknown information to provide good cause for STM's belated identification of claims. STM was simply laying behind the log until the eve of P.R. 4–1 disclosures —***after*** Motorola produced documents in view of the original claims and ***after*** Motorola's invalidity contentions were made and then elected to disregard the Court's rules. Motorola had only 7 days, instead of the Court ordered 42 days, to analyze the 26 new claims before P.R. 4–1 disclosures were due. This tactical gamesmanship should not be permitted. Indeed, Patent Rule 3-7 was designed to deter such

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[13] Letter from Hilda Galvan to Bruce Sostek dated December 5, 2003 (Ex. H).

[14] Notice of Scheduling Conference, Proposed Dates for Docket Control Order, and Discovery Order dated September 29, 2003, at 7.

gamesmanship by requiring the parties to seek leave and to show good cause in order to supplement any preliminary contentions.

Motorola files this motion in order to require STM to comply with the patent rules and to establish for all parties that those rules will be enforced by this Court. Accordingly, Motorola requests that the Court (1) strike STM's First Supplement to Disclosure of Asserted Claims and Preliminary Infringement Contentions and (2) require STM to comply with Patent Rule 3–7 of the Court's order by seeking leave to amend their infringement contentions and showing good cause to do so.

Dated: December 18, 2003

Respectfully submitted,

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ATTORNEYS FOR DEFENDANT MOTOROLA, INC.

[15] *See, e.g.*, Ex. A at Exhibit B-1 (claim 23) and Ex. G at Page B-4 (claim 1) (containing identical descriptions of where each element of claim 26 (original contentions) and claim 1 (newly-added) are allegedly found in Motorola's DSP56305 product).

CERTIFICATE OF CONFERENCE

The undersigned does hereby certify that counsel has conferred with opposing counsel in a good faith attempt to resolve the above-stated matter without court intervention. STM is opposed to Motion To Enforce Paragraph 3–7 of the Court's Patent Rules

Kenneth Adamo by pem.
Attorney for Defendant and Counterclaim
Plaintiff Motorola, Inc.

CERTIFICATE OF SERVICE

I hereby certify that on this 18th day of December, 2003, a true and correct copy of the above and foregoing document has been forwarded via Federal Express to the following counsel:

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Exhibit "A"

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
SHERMAN DIVISION

STMICROELECTRONICS, INC., Plaintiff, vs. MOTOROLA, INC., Defendant.	CIVIL ACTION NO. 4:03–CV–276

DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS OF PLAINTIFF STMICROELECTRONICS, INC.

Plaintiff STMicroelectronics, Inc. ("ST INC"), by and through its attorneys, makes this Disclosure of Asserted Claims and Preliminary Infringement Contentions, pursuant to local Patent Rule 3–1. The asserted claims and infringement contentions, with the accompanying exhibits, are not intended to reflect, nor should they be construed to include, any other contentions.

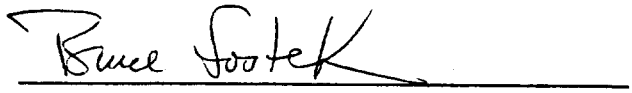
ST INC's infringement contentions are preliminary in that they reflect ST INC's knowledge and contentions as of this date in the present action. Accordingly, ST INC reserves the right to modify and supplement, without prejudice, its Disclosure of Asserted Claims and Preliminary Infringement Contentions, including but not limited to claims asserted, products accused, and bases for the asserted infringement.

ST INC's infringement contentions regarding U.S. Patent No. 5,812,789 are attached hereto as Exhibit A. ST INC's infringement contentions regarding U.S. Patent No. 5,031,092

12/18/03

are attached as Exhibit B. ST INC's infringement contentions regarding U.S. Patent No. 5,359,244 are attached as Exhibit C.

Respectfully submitted,



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ATTORNEYS FOR PLAINTIFF
STMICROELECTRONICS, INC.

CERTIFICATE OF SERVICE

On the 31st day of October, 2003, a copy of the foregoing was served upon the following counsel of record as indicated:

Via Overnight Delivery

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EXHIBIT A

DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS OF PLAINTIFF STMICROELECTRONICS, INC. FOR U.S. PATENT NO. 5,812,789

ST INC makes the following infringement contentions with respect to U.S. Patent No. 5,812,789 (the "'789 patent"):

3–1(a) Each claim of each patent in suit that is allegedly infringed by each opposing party:

ST INC asserts that Motorola infringes at least Claim 1.

3–1(b) Separately for each asserted claim, each accused apparatus, product, device, process, method, act or other instrumentality ("Accused Instrumentality") of each opposing party of which the party is aware. This identification shall be as specific as possible. Each product, device, and apparatus must be identified by name or model number, if known. Each method or process must be identified by name, if known, or by any product, device or apparatus which, when used, allegedly results in the practice of the claimed method or process:

ST INC asserts that Claim 1 is infringed by the products identified below:

Motorola Products that Infringe Claim 1
MCT4000 Transport and Video Processor
MCT4100 Transport and Video Processor
MCT5100 M–DTV Module
RD2 Reference Design Platform

3–1(c) A chart identifying specifically where each element of each asserted claim is found within each Accused Instrumentality, including for each element that such party contends is governed by 35 U.S.C. § 112(6), the identity of the structure(s), act(s), or material(s) in the Accused Instrumentality that performs the claimed function:

The chart for each identified product is included at the identified Exhibit:

Infringing Motorola Product	Exhibit No.
MCT4000 Transport and Video Processor	A–1
MCT4100 Transport and Video Processor	A–2
MCT5100 M–DTV Module	A–3
RD2 Reference Design Platform	A–4

3–1(d) Whether each element of each asserted claim is claimed to be literally present or present under the doctrine of equivalents in the Accused Instrumentality:

Presently, ST INC believes that each element of each asserted claim is literally found in the accused products as described in the accompanying exhibits, but ST INC reserves the right to assert infringement under the doctrine of equivalents after further investigation and/or construction of claim terms by the Court.

3–1(e) For any patent that claims priority to an earlier application, the priority date to which each asserted claim allegedly is entitled:

The '789 patent claims a priority date of August 26, 1996.

3–1(f) If a party claiming patent infringement wishes to preserve the right to rely, for any purpose, on the assertion that its own apparatus, product, device, process, method, act, or other instrumentality practices the claimed invention, the party must identify, separately for each asserted claim, each such apparatus, product, device, process, method, act, or other instrumentality that incorporates or reflects that particular claim:

Presently, ST INC is not relying on the assertion that its own apparatus, product, device, process, method, act, or other instrumentality practices the claimed invention.

EXHIBIT A–1

Claim 1 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT4000 Transport and Video Processor**
1. An electronic system	MCT4000 Reference Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram;
coupled to a memory, comprising:	MCT4000 Reference Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram, "4MB SDRAM Video Memory";
a first device that requires access to the memory;	MCT4000 Reference Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram, "MPC850 Host Processor"; MCT4000 Reference Manual at page 4, paragraph 1.4.1 "–supports DMA access to/from MCT4000's External Memory";
a decoder that requires access to the memory	MCT4000 Reference Manual at page 3, Fig. 1–2, MCT4000 Block Diagram, "Video Decoder";
sufficient to maintain real time operation; and	MCT4000 Reference Manual at page 147, paragraph 9.2.1 "real time";
a memory interface for coupling to the memory, and coupled to the first device and to the decoder,	MCT4000 Reference Manual at page 3, Fig. 1–2, MCT4000 Block Diagram, "Memory Controller";
the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory	MCT4000 Reference Manual at page 145, paragraph 9.1 "All SDRAM accesses are controlled by the memory controller."; MCT4000 Reference Manual at page 151, paragraph 9.3.2 "The MC [Memory Controller] stores one 'on deck' request in a register which holds the address, size and client ID information. Priority among competing clients is exercised at the time of reading the data into this 'ready register'";
and a shared bus coupled to the memory the first device, and the decoder, the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.	MCT4000 Reference Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram; "data" and "address & control" buses coupling the MCT4000 and the video memory.

EXHIBIT A–2

Claim 1 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT4100 Transport and Video Processor**
1. An electronic system	Cadence Design Systems, Inc. *Customer Success*, Reference 804, Motorola – Entertainment Solutions Division at page 2 "...the MCT4100 with MCT4000 functionality ..." MCT4000 Reference Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram;
coupled to a memory, comprising:	MCT4000 Reference Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram, "4MB SDRAM Video Memory";
a first device that requires access to the memory;	MCT4000 Reference Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram, "MPC850 Host Processor"; MCT4000 Reference Manual at page 4, paragraph 1.4.1 "–supports DMA access to/from MCT4000's External Memory";
a decoder that requires access to the memory	MCT4000 Reference Manual at page 3, Fig. 1–2, MCT4000 Block Diagram, "Video Decoder";
sufficient to maintain real time operation; and	MCT4000 Reference Manual at page 147, paragraph 9.2.1 "real time";
a memory interface for coupling to the memory, and coupled to the first device and to the decoder,	MCT4000 Reference Manual at page 3, Fig. 1–2, MCT4000 Block Diagram, "Memory Controller";
the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory	MCT4000 Reference Manual at page 145, paragraph 9.1 "All SDRAM accesses are controlled by the memory controller."; MCT4000 Reference Manual at page 151, paragraph 9.3.2 "The MC [Memory Controller] stores one 'on deck' request in a register which holds the address, size and client ID information. Priority among competing clients is exercised at the time of reading the data into this 'ready register'";
and a shared bus coupled to the memory the first device, and the decoder, the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.	MCT4000 Reference Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram; "data" and "address & control" buses coupling the MCT4000 and the video memory.

EXHIBIT A–3

Claim 1 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT5100 M–DTV Module**
1. An electronic system	Sampo Corporation Press Release: *Sampo Corporation Declares Motorola's M–DTV™ Module of Choice for Digital TV-Enabled Sets* at page 1 "The MCT5100 M–DTV module integrates ...an MPEG decoder and controller ... The MCT4000 is also included in this module ..." MCT4000 Reference Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram;
coupled to a memory, comprising:	MCT4000 Reference Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram, "4MB SDRAM Video Memory";
a first device that requires access to the memory;	MCT4000 Ref. Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram, "MPC850 Host Processor"; MCT4000 Reference Manual at page 4, paragraph 1.4.1 "–supports DMA access to/from MCT4000's External Memory";
a decoder that requires access to the memory	MCT4000 Reference Manual at page 3, Fig. 1–2, MCT4000 Block Diagram, "Video Decoder";
sufficient to maintain real time operation; and	MCT4000 Reference Manual at page 147, paragraph 9.2.1 "real time";
a memory interface for coupling to the memory, and coupled to the first device and to the decoder,	MCT4000 Reference Manual at page 3, Fig. 1–2, MCT4000 Block Diagram, "Memory Controller";
the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory	MCT4000 Reference Manual at page 145, paragraph 9.1 "All SDRAM accesses are controlled by the memory controller."; MCT4000 Reference Manual at page 151, paragraph 9.3.2 "The MC [Memory Controller] stores one 'on deck' request in a register which holds the address, size and client ID information. Priority among competing clients is exercised at the time of reading the data into this 'ready register'";
and a shared bus coupled to the memory the first device, and the decoder, the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.	MCT4000 Reference Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram; "data" and "address & control" buses coupling the MCT4000 and the video memory.

EXHIBIT A–4

Claim 1 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's RD2 Reference Design Platform**
1. An electronic system	January 30, 1999 Press Release *First Collaboration of Motorola and Sarnoff Culminates in Cost-Effective Semiconductor Solution Offering for the DTV Market*, at page 1 "The RD2 features Motorola's popular MCP850 PowerPC™ processor .... Also featured are Motorola's MCT4000 ..." MCT4000 Reference Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram;
coupled to a memory, comprising:	MCT4000 Reference Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram, "4MB SDRAM Video Memory";
a first device that requires access to the memory;	MCT4000 Ref. Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram, "MPC850 Host Processor"; MCT4000 Reference Manual at page 4, paragraph 1.4.1 "–supports DMA access to/from MCT4000's External Memory";
a decoder that requires access to the memory	MCT4000 Reference Manual at page 3, Fig. 1–2, MCT4000 Block Diagram, "Video Decoder";
sufficient to maintain real time operation; and	MCT4000 Reference Manual at page 147, paragraph 9.2.1 "real time";
a memory interface for coupling to the memory, and coupled to the first device and to the decoder,	MCT4000 Reference Manual at page 3, Fig. 1–2, MCT4000 Block Diagram, "Memory Controller";
the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory	MCT4000 Reference Manual at page 145, paragraph 9.1 "All SDRAM accesses are controlled by the memory controller."; MCT4000 Reference Manual at page 151, paragraph 9.3.2 "The MC [Memory Controller] stores one 'on deck' request in a register which holds the address, size and client ID information. Priority among competing clients is exercised at the time of reading the data into this 'ready register'";
and a shared bus coupled to the memory the first device, and the decoder, the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.	MCT4000 Reference Manual at page 2, Fig. 1–1, SDTV Processor Block Diagram; "data" and "address & control" buses coupling the MCT4000 and the video memory.

EXHIBIT B

DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS OF PLAINTIFF STMICROELECTRONICS, INC. FOR U.S. PATENT NO. 5,031,092

ST INC makes the following infringement contentions with respect to U.S. Patent No. 5,031,092 (the "'092 patent"):

3–1(a) Each claim of each patent in suit that is allegedly infringed by each opposing party:

ST INC asserts that Motorola infringes at least Claim 23.

3–1(b) Separately for each asserted claim, each accused apparatus, product, device, process, method, act or other instrumentality ("Accused Instrumentality") of each opposing party of which the party is aware. This identification shall be as specific as possible. Each product, device, and apparatus must be identified by name or model number, if known. Each method or process must be identified by name, if known, or by any product, device or apparatus which, when used, allegedly results in the practice of the claimed method or process:

ST INC asserts that Claim 23 is infringed by the products identified below:

Motorola Products that Infringe Claim 23
DSP56305 24–Bit Digital Signal Processor
DSP56F801/803/805/807 16–Bit Digital Signal Processors
DSP56321 24–Bit Digital Signal Processor
DSP56362 24–Bit Digital Signal Processor
MC68332 32–Bit Microcontroller
MC68336 and MC68376 32–Bit Microcontrollers
MPC555 and MPC556 RISC Microcontrollers
MPC565 and MPC566 RISC Microcontrollers
MPC7410 RISC Microprocessor
MPC7441/7445 and MPC7450/7451/7455 RISC Microprocessors

3–1(c) A chart identifying specifically where each element of each asserted claim is found within each Accused Instrumentality, including for each element that such party contends is governed by 35 U.S.C. § 112(6), the identity of the structure(s), act(s), or material(s) in the Accused Instrumentality that performs the claimed function:

The chart for each identified product is included at the identified Exhibit:

Infringing Motorola Product	Exhibit No.
DSP56305 24–Bit Digital Signal Processor	B–1
DSP56F801/803/805/807 16–Bit Digital Signal Processors	B–2
DSP56321 24–Bit Digital Signal Processor	B–3
DSP56362 24–Bit Digital Signal Processor	B–4
MC68332 32–Bit Microcontroller	B–5
MC68336 and MC68376 32–Bit Microcontrollers	B–6
MPC555 and MPC556 RISC Microcontrollers	B–7
MPC565 and MPC566 RISC Microcontrollers	B–8
MPC7410 RISC Microprocessor	B–9
MPC7441/7445 and MPC7450/7451/7455 RISC Microprocessors	B–10

3–1(d) Whether each element of each asserted claim is claimed to be literally present or present under the doctrine of equivalents in the Accused Instrumentality:

Presently, ST INC believes that each element of each asserted claim is literally found in the accused products as described in the accompanying exhibits, but ST INC reserves the right to assert infringement under the doctrine of equivalents after further investigation and/or construction of claim terms by the Court.

3–1(e) For any patent that claims priority to an earlier application, the priority date to which each asserted claim allegedly is entitled:

Claim 23 of the '092 patent claims a priority date of November 16, 1983.

3–1(f) If a party claiming patent infringement wishes to preserve the right to rely, for any purpose, on the assertion that its own apparatus, product, device, process, method, act, or other instrumentality practices the claimed invention, the party must identify, separately for each asserted claim, each such apparatus, product, device, process, method, act, or other instrumentality that incorporates or reflects that particular claim:

Presently, ST INC is not relying on the assertion that its own apparatus, product, device, process, method, act, or other instrumentality practices the claimed invention.

EXHIBIT B–1

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56305 24–Bit Digital Signal Processor**
23. A microcomputer comprising	DSP56305 User's Manual at page 1–3, paragraph 1.1 "This manual describes the DSP56305 24–bit Digital Signal Processor (DSP), its memory, operating modes and peripheral modules.";
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56305 User's Manual at page 1–14, Fig. 1–1 DSP56305 Block Diagram, "24–Bit DSP56300 Core";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	DSP56305 User's Manual at page 1–14, Fig. 1–1 DSP56305 Block Diagram, "P Memory RAM 6.5K x 24";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56305 User's Manual at page 1–14, Fig. 1–1 DSP56305 Block Diagram, "P Memory RAM 6.5K x 24";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	DSP56305 User's Manual at page 1–14, Fig. 1–1 DSP56305 Block Diagram, "Program Address Generator";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	DSP56305 User's Manual at page 1–14, Paragraph 1.8 "Program Data Bus (PDB)"";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56305 User's Manual at page 1–14, Fig. 1–1 DSP56305 Block Diagram, "Program Decoder Controller";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	DSP56305 User's Manual at page 1–14, Fig. 1–1 DSP56305 Block Diagram, "Data ALU 24 x 24*56 ->56–bit MAC";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	On information and belief, the "P Memory RAM 6.5K x 24" resides in a first isolation region;

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56305 24–Bit Digital Signal Processor**
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	On information and belief, some of the transistors of the, "Data ALU 24 x 24*56 –>56–bit MAC" reside in a second isolation region;
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

EXHIBIT B–2

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16–Bit Digital Signal Processors**
23. A microcomputer comprising	DSP56F801/803/805/807 User's Manual; at page 1–3, paragraph 1.1 "Combined on a single chip are the processing power of a DSP and the functionality of a micro controller and a flexible set of peripherals."
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56F801/803/805/807 User's Manual; at page 1–19. Fig. 1–6 "DSP 16–Bit Core";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	DSP56F801/803/805/807 User's Manual; at page 1–15, Table 1–2 "Program RAM" 1K x 16 (DSP56F801), 512 x 16 (DSP56F803), 512 x 16 (DSP56F805), 2K x 16 (DSP56F807);
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56F801/803/805/807 User's Manual; at page 1–15, Table 1–2 "Program RAM" 1K x 16 (DSP56F801), 512 x 16 (DSP56F803), 512 x 16 (DSP56F805), 2K x 16 (DSP56F807) and page 1–18 Fig. 1–5 "Program Memory";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	DSP56F801/803/805/807 User's Manual at page 1–18, Fig. 1–5 "Program Controller [PC]";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	DSP56F801/803/805/807 User's Manual at page 1–23, Table 1–3 ""PDB Program Data Bus 16–bit bi-directional, instruction word fetches";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56F801/803/805/807 User's Manual at page 1–18, Fig. 1–5 "Instr. Decoder";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	DSP56F801/803/805/807 User's Manual at page 1–18, Fig. 1–5 "Data ALU" and Motorola DSP56F803 Die Images [Substrate Level, @ ~1200x];

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16–Bit Digital Signal Processors
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	Motorola DSP56F803 Die Images [Substrate Level, @ ~35x], [Substrate Level @ ~200x] and [Substrate Level @ ~1200x];
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	Motorola DSP56F803 Die Images [Substrate Level, @ ~200x] and [Substrate Level @ ~1200x];
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola DSP56F803 Die Images [Substrate Level, @ ~1200x].

EXHIBIT B–3

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56321 24–Bit Digital Signal Processor**
23. A microcomputer comprising	DSP56321 Reference Manual 24–Bit Digital Signal Processor;
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56321 Reference Manual at page 1–11, Fig. 1–1 DSP56321 Block Diagram, "24–Bit DSP56300 Core";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	DSP56321 Reference Manual at page 1–11, Fig. 1–1 DSP56321 Block Diagram, "Program RAM 32K x 24 bit";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56321 Reference Manual at page 1–11, Fig. 1–1 DSP56321 Block Diagram, "Program RAM 32K x 24 bit";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	DSP56321 Reference Manual at page 1–11, Fig. 1–1 DSP56321 Block Diagram, "Program Address Generator";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	DSP56321 Reference Manual at page 1–11, Fig. 1–1 DSP56321 Block Diagram, "PDB" and page 1–10, paragraph 1.6 "Program data bus for carrying program data throughout the core";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56321 Reference Manual at page 1–11, Fig. 1–1 DSP56321 Block Diagram, "Program Decode Controller";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	DSP56321 Reference Manual at page 1–11, Fig. 1–1 DSP56321 Block Diagram, "Data ALU 24 x 24*56 ->56–bit MAC";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	On information and belief, the "Program RAM 32K x 24 bit" resides in a first isolation region;

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56321 24–Bit Digital Signal Processor**
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	On information and belief, some of the transistors of the "Data ALU 24 x 24*56 –>56–bit MAC" reside in a second isolation region;
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

EXHIBIT B–4

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56362 24–Bit Digital Signal Processor**
23. A microcomputer comprising	DSP56362 Reference Manual at page 1–1, paragraph 1.1 "This manual describes the DSP56362 24–bit digital signal processor (DSP), its memory, operating modes and peripheral modules.";
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56362 Reference Manual at page 1–3, Fig. 1–1 DSP56362 Block Diagram, "24–bit DSP56300 Core";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	DSP56362 Reference Manual at page 1–3, Fig. 1–1 DSP56362 Block Diagram, "Program RAM Instr. Cache 3K x 24";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56362 Reference Manual at page 1–3, Fig. 1–1 DSP56362 Block Diagram, "Program RAM Instr. Cache 3K x 24";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	DSP56362 Reference Manual at page 1–3, Fig. 1–1 DSP56362 Block Diagram, "Program Address Generator";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	DSP56362 Reference Manual at page 1–3, Fig. 1–1 DSP56362 Block Diagram, "PDB" and page 1–7, paragraph 1.4.4 "Program Data Bus (PDB) for carrying program data throughout the core";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56362 Reference Manual at page 1–3, Fig. 1–1 DSP56362 Block Diagram, "Program Decode Controller";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	DSP56362 Reference Manual at page 1–3, Fig. 1–1 DSP56362 Block Diagram, "Data ALU 24 x 24*56 –> 56–bit MAC ";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	On information and belief, the "Program RAM Instr. Cache 3K x 24" resides in a first isolation region;

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56362 24–Bit Digital Signal Processor**
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	On information and belief, some of the transistors of the "Data ALU 24 x 24*56 –>56–bit MAC" reside in a second isolation region;
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

EXHIBIT B–5

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller**
23. A microcomputer comprising	MC68332 User's Manual, page 3–3, Fig. 3–1 MC68332 Block Diagram "MC68332";
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MC68332 User's Manual, page 3–3, Fig. 3–1 MC68332 Block Diagram "TPU" and page 7–1 Section 7 "time processor unit (TPU)"; TPU Time Processor Unit Reference Manual, page 4–2, Fig. 4–1 TPU Detailed Block Diagram "TPU";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	MC68332 User's Manual, page 3–3, Fig. 3–1 MC68332 Block Diagram "2K TPURAM" and page 3–2, paragraph 3.1.5 "2 Kbytes of static RAM";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MC68332 User's Manual, page 3–3, Fig. 3–1 MC68332 Block Diagram "2K TPURAM" and page 3–2, paragraph 3.1.5 "2 Kbytes of static RAM"; TPU Time Processor Unit Reference Manual, page 4–19, paragraph 4.2.10 "load microcode into the RAM",
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual, page 4–2, Fig. 4–1 TPU Detailed Block Diagram "uPC" and page 4–14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	TPU Time Processor Unit Reference Manual, page 4–2, Fig. 4–1 TPU Detailed Block Diagram "Microinstruction Register" and page 4–18, paragraph 4.2.8 "The 32–bit register contains the microinstruction currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual, page 4–8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions.";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	MC68332 User's Manual, page 3–3, Fig. 3–1 MC68332 Block Diagram "CPU32"; Motorola MC68332 Die Image [Substrate Level @ ~800x].
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	Motorola MC68332 Die Image [Poly Level, @ ~30x], [Substrate Level @ ~50x] and [Substrate Level @ ~800x];

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller**
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	Motorola MC68332 Die Image [Substrate Level @ ~800x];
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MC68332 Die Image [Substrate Level @ ~800x].

EXHIBIT B–6

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MC68336 and MC68376 32–Bit Microcontrollers**
23. A microcomputer comprising	MC68336/376 User's Manual at page 3–4, Fig. 3–1 MC68336/376 Block Diagram "MC68336/376";
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MC68336/376 User's Manual at page 3–4, Fig. 3–1 MC68336/376 Block Diagram "TPU" and page 11–1 Section 11 "time processor unit (TPU)"; TPU Time Processor Unit Reference Manual at page 4–2, Fig. 4–1 TPU Detailed Block Diagram "TPU";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	MC68336/376 User's Manual at page 3–4, Fig. 3–1 MC68336/376 Block Diagram "3.5 KBYTE TPURAM" and page 3.2 paragraph 3.1.9 "3.5 Kbytes of static RAM";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MC68336/376 User's Manual at page 3–4, Fig. 3–1 MC68336/376 Block Diagram "3.5 KBYTE TPURAM"; TPU Time Processor Unit Reference Manual at page 4–19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4–2, Fig. 4–1 TPU Detailed Block Diagram "uPC" and page 4–14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	TPU Time Processor Unit Reference Manual at page 4–2, Fig. 4–1 TPU Detailed Block Diagram "Microinstruction Register" and page 4–18, paragraph 4.2.8 "The 32–bit register contains the microinstruction currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4–8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	MC68336/376 User's Manual at page 3–4, Fig. 3–1 MC68336/376 Block Diagram "CPU32"; Motorola MC68336 Die Image [Substrate Level, @ ~800x];

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MC68336 and MC68376 32-Bit Microcontrollers**
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	Motorola MC68336 Die Image [Poly Level, @ ~20x], [Substrate Level, @ ~70x] and [Substrate Level, @ ~800x];
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	Motorola MC68336 Die Image [Substrate Level, @ ~800x];
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MC68336 Die Image [Substrate Level, @ ~800x];

EXHIBIT B–7

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC555 and MPC556 RISC Microcontrollers**
23. A microcomputer comprising	MPC555/MPC556 User's Manual at page 1–2, Fig. 1–1 MPC555/MPC556 Block Diagram "MPC555/MPC556";
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC555/MPC556 User's Manual at page 1–2, Fig. 1–1 MPC555/MPC556 Block Diagram "TPU3", page 1–4 paragraph 1.2.8 "Two Time Processor Units (TPU3)" and page 17–1 Section 17 "time processor unit 3 (TPU3)"; TPU Time Processor Unit Reference Manual at page 4–2, Fig. 4–1 TPU Detailed Block Diagram "TPU";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	MPC555/MPC556 User's Manual at page 1–2, Fig. 1–1 MPC555/MPC556 Block Diagram "DPTRAM" and page 1–4 paragraph 1.2.8 "6–Kbyte dual port TPU RAM ... for TPU microcode"; Motorola MPC555 Die Image [Poly Level, @ ~15x]
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC555/MPC556 User's Manual at page 1–2, Fig. 1–1 MPC555/MPC556 Block Diagram "DPTRAM" and page 1–4 paragraph 1.2.8 "6–Kbyte dual port TPU RAM ... for TPU microcode"; TPU Time Processor Unit Reference Manual at page 4–19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4–2, Fig. 4–1 TPU Detailed Block Diagram "uPC" and page 4–14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	TPU Time Processor Unit Reference Manual at page 4–2, Fig. 4–1 TPU Detailed Block Diagram "Microinstruction Register" and page 4–18, paragraph 4.2.8 "The 32–bit register contains the microinstructions currently being executed.";

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC555 and MPC556 RISC Microcontrollers**
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4–8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	MPC555/MPC556 User's Manual at page 1–2, Fig. 1–1 MPC555/MPC556 Block Diagram "192 Kbytes Flash"; Motorola MPC555 Die Image [Substrate Level @ ~800x];
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	Motorola MPC555 Die Image [Poly Level, @ ~15x], [Substrate Level, @ ~50x] and [Substrate Level @ ~800x];
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	Motorola MPC555 Die Image [Substrate Level @ ~800x];
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MPC555 Die Image [Substrate Level @ ~800x].

EXHIBIT B–8

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers**
23. A microcomputer comprising	MPC565/MPC566 Reference Manual at page 1–2, Fig. 1–1 MPC565/MPC566 Block Diagram "MPC565/MPC566";
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC565/MPC566 Reference Manual at page 1–2, Fig. 1–1 MPC565/MPC566 Block Diagram "TPU3" and page 18–1, Section 18 "The time processor unit 3 (TPU3), an enhanced version of the original TPU…"; TPU Time Processor Unit Reference Manual at page 4–2, Fig. 4–1 TPU Detailed Block Diagram "TPU";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	MPC565/MPC566 Reference Manual at page 1–2, Fig. 1–1 MPC565/MPC566 Block Diagram "4 Kbytes DPTRAM";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC565/MPC566 Reference Manual at page 1–2, Fig. 1–1 MPC565/MPC566 Block Diagram "4 Kbytes DPTRAM" and page 1–4 "… the 4–Kbyte dedicated to the third TPU3 for microcode"; TPU Time Processor Unit Reference Manual at page 4–19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4–2, Fig. 4–1 TPU Detailed Block Diagram "uPC" and page 4–14, paragraph 4.2.3 "The uPC contains the address used to access a microword …";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	TPU Time Processor Unit Reference Manual at page 4–2, Fig. 4–1 TPU Detailed Block Diagram "Microinstruction Register" and page 4–18, paragraph 4.2.8 "The 32–bit register contains the microinstructions currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4–8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers**
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	MPC565/MPC566 Reference Manual at page 1–2, Fig. 1–1 MPC565/MPC566 Block Diagram "PowerPC Core";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	On information and belief, the "4 Kbytes DPTRAM" resides in a first isolation region;
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	On information and belief, some of the transistors of the, "PowerPC Core" reside in a second isolation region;
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

EXHIBIT B–9

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor**
23. A microcomputer comprising	MPC7410 RISC Microprocessor User's Manual at page 1–1, Paragraph 1.1 "MPC7410";
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC7410 RISC Microprocessor User's Manual at page 1–4, Fig. 1–1 MPC7410 Microprocessor Block Diagram "Branch Processing Unit" and page 6–22, paragraph 6.4.1 "Branch Processing Unit";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	MPC7410 RISC Microprocessor User's Manual at page 1–4, Fig. 1–1 MPC7410 Microprocessor Block Diagram "32–Kbyte I Cache";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC7410 RISC Microprocessor User's Manual at page 1–4, Fig. 1–1 MPC7410 Microprocessor Block Diagram "32–Kbyte I Cache" and page 3–1, Chapter 3 "The MPC7410 microprocessor contains separate 32–Kbyte ... instruction and data caches ...";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	MPC7410 RISC Microprocessor User's Manual at page 1–4, Fig. 1–1 MPC7410 Microprocessor Block Diagram "Fetcher" and page 1–9, paragraph 1.2.2 "The sequential fetcher loads instructions from the instruction cache ...";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	MPC7410 RISC Microprocessor User's Manual at page 1–4, Fig. 1–1 MPC7410 Microprocessor Block Diagram "Instruction Queue" and page 1–10, paragraph 1.2.2.1 "The instruction queue (IQ) ... holds as many as six instructions ...";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	MPC7410 RISC Microprocessor User's Manual at page 1–4, Fig. 1–1 MPC7410 Microprocessor Block Diagram "Dispatch Unit" and page 6–6 "The decode/dispatch stage consists of the time it takes to fully decode the instruction ...";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	MPC7410 RISC Microprocessor User's Manual at page 1–4, Fig. 1–1 MPC7410 Microprocessor Block Diagram "32–Kbyte D Cache" and page 1–2 "The MPC7410 has independent on-chip 32–Kbyte, eight-way, set associative, physically-addressed L1 (level-one) caches for instructions and data ..."; Motorola MPC7410 Die Image [Substrate Level, @ ~1200x];

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor**
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x];
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x];
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x].

EXHIBIT B–10

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors**
23. A microcomputer comprising	MPC7450 RISC Microprocessor Family User's Manual at page 1–5, Paragraphs 1.1.1 through 1.1.4 "MPC7441", "MPC7450", "MPC7455" and "MPC7445" respectively;
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC7450 RISC Microprocessor Family User's Manual at page 1–4, Fig. 1–1 MPC7451 Microprocessor Block Diagram "Branch Processing Unit" and page 1–13, paragraph 1.2.2.2 "Branch Processing Unit";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	MPC7450 RISC Microprocessor Family User's Manual at page 1–4, Fig. 1–1 MPC7451 Microprocessor Block Diagram "32–Kbyte I Cache" and page 1–17, paragraph 1.2.4 "The MPC7451 implements separate L1 instruction and data caches. Each cache is 32–Kbyte …";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC7450 RISC Microprocessor Family User's Manual at page 1–4, Fig. 1–1 MPC7451 Microprocessor Block Diagram "32–Kbyte I Cache" and page 1–17, paragraph 1.2.4 "The MPC7451 implements separate L1 instruction and data caches. Each cache is 32–Kbyte …" ;
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	MPC7450 RISC Microprocessor Family User's Manual at page 1–4, Fig. 1–1 MPC7451 Microprocessor Block Diagram "Fetcher" and page 1–12, paragraph 1.2.2 "The sequential fetcher loads instructions from the instruction cache …";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	MPC7450 RISC Microprocessor Family User's Manual at page 1–4, Fig. 1–1 MPC7451 Microprocessor Block Diagram "Instruction Queue" and page 1–12, paragraph 1.2.2 "The instruction queue (IQ) … holds as many as 12 instructions …";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	MPC7450 RISC Microprocessor Family User's Manual at page 1–4, Fig. 1–1 MPC7451 Microprocessor Block Diagram "Dispatch Unit" and page 1–53 "The decode/dispatch stage fully decodes each instruction …";

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	MPC7450 RISC Microprocessor Family User's Manual at page 1–4, Fig. 1–1 MPC7451 Microprocessor Block Diagram "Integer Unit 1";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	On information and belief, the "32–Kbyte I Cache" resides in a first isolation region;
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	On information and belief, some of the transistors of the "Integer Unit 1" reside in a second isolation region;
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

EXHIBIT C

DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS OF PLAINTIFF STMICROELECTRONICS, INC. FOR U.S. PATENT NO. 5,359,244

ST INC makes the following infringement contentions with respect to U.S. Patent No. 5,359,244 (the "'244 patent"):

3–1(a) Each claim of each patent in suit that is allegedly infringed by each opposing party:

ST INC asserts that Motorola infringes at least Claims 1, 13, 14 and 15.

3–1(b) Separately for each asserted claim, each accused apparatus, product, device, process, method, act, or other instrumentality ("Accused Instrumentality") of each opposing party of which the party is aware. This identification shall be as specific as possible. Each product, device, and apparatus must be identified by name or model number, if known. Each method or process must be identified by name, if known, or by any product, device, or apparatus which, when used, allegedly results in the practice of the claimed method or process:

ST INC asserts that Claim 1 is infringed by the products identified below:

Motorola Products that Infringe Claim 1
MC33253
MC33883

ST INC asserts that Claim 13 is infringed by the products identified below:

Motorola Products that Infringe Claim 13
MC33253

ST INC asserts that Claim 14 is infringed by the products identified below:

Motorola Products that Infringe Claim 14
MC33253
MC33883

ST INC asserts that Claim 15 is infringed by the products identified below:

Motorola Products that Infringe Claim 15
MC33253
MC33883

3–1(c) A chart identifying specifically where each element of each asserted claim is found within each Accused Instrumentality, including for each element that such party contends is governed by 35 U.S.C. §112(6), the identity of the structure(s), act(s), or material(s) in the Accused Instrumentality that performs the claimed function:

The chart for each identified product is included at the identified Exhibit:

Infringing Motorola Product	Exhibit No.
MC33253	C–1
MC33883	C–2

3–1(d) Whether each element of each asserted claim is claimed to be literally present or present under the doctrine of equivalents in the Accused Instrumentality:

Presently, ST INC believes that each element of each asserted claim is literally found in the accused products as described in the accompanying exhibits, but ST INC reserves the right to assert infringement under the doctrine of equivalents after further investigation and/or construction of claim terms by the Court.

3–1(e) For any patent that claims priority to an earlier application, the priority date to which each asserted claim allegedly is entitled:

The '244 patent claims a priority date of July 31, 1992.

3–1(f) If a party claiming patent infringement wishes to preserve the right to rely, for any purpose, on the assertion that its own apparatus, product, device, process, method, act, or other instrumentality practices the claimed invention, the party must identify, separately for each asserted claim, each such apparatus, product, device, process, method, act, or other instrumentality that incorporates or reflects that particular claim:

Presently, ST INC is not relying on the assertion that its own apparatus, product, device, process, method, act, or other instrumentality practices the claimed invention.

EXHIBIT C–1

Claim 1 of U.S. Patent No. 5,359,244	
Claim Language	**Description of where each claim element is found in Motorola's MC33253**
A circuit for driving a MOS power transistor, comprising:	Motorola's data sheet, designated "order number: MC33253/D" (herein the "Data Sheet") describes that the MC33253 is a "pre-driver." It drives a MOS power transistor.
a first gate drive circuit for charge pumping a node connected to a gate of the MOS power transistor to a gate supervoltage higher than a positive supply voltage by at least an amount equal to a threshold voltage of the MOS power transistor, wherein the first gate drive circuit utilizes a first charge current to charge the MOS power transistor gate to the gate supervoltage at a first rate;	The Data Sheet includes a Figure 1 showing the "Principal Building Blocks" of the MC33253. Figure 1 contains a block labeled "Charge Pump" that is connected to the gate of the MOS power transistor through a block labeled "Output." Within these blocks is a circuit that generates a first current of up to 1A at the output designated GATE_HS.
a second gate drive circuit for charge pumping the node connected to the gate of the MOS power transistor to maintain the voltage on such node at the gate supervoltage, wherein the second gate drive circuit utilizes a second charge current, less than the first charge current, to charge the MOS power transistor gate to the gate supervoltage at a second rate which is slower than the first rate; and	The Data Sheet includes a Figure 1 showing the "Principal Building Blocks" of the MC33253. Figure 1 contains a block labeled "Charge Pump" that is connected to the gate of the MOS power transistor through a block labeled "Output." Upon information and belief, within these blocks is a circuit that generates a second current of up to 100mA at the output designated GATE_HS.
a control circuit, wherein the control circuit enables the first and second gate drive circuits when the MOS power transistor is initially turned on, and thereafter disables the first gate drive circuit after a selected period of time.	The Data Sheet includes a Figure 1 showing the "Principal Building Blocks" of the MC33253. Figure 1 contains a block labeled "Logic" connected through other blocks to the output block. Upon information and belief, within these blocks is a control circuit.

Claim 13 of U.S. Patent No. 5,359,244	
Claim Language	**Description of where each claim element is found in Motorola's MC33253**
The circuit of claim 1,	See description above for claim 1.
further comprising means for connecting the gate of the MOS power transistor to ground, wherein the MOS power transistor can be turned off when desired.	The Data Sheet includes a Figure 8 that shows a transistor T2 that acts as a switch to complete a low resistance path to ground to turn off the gate of the MOS power transistor when desired.

Claim 14 of U.S. Patent No. 5,359,244	
Claim Language	**Description of where each claim element is found in Motorola's MC33253**
A method for driving a MOS power transistor, comprising the steps of:	As described above in connection with claim 1, the MC33253 drives a MOS power transistor. When the device operates, it performs a method for driving a MOS power transistor.
when the MOS power transistor is turned on, charging a node connected to a gate thereof to a gate supervoltage higher than a positive supply voltage by at least an amount equal to a threshold voltage of the MOS power transistor, utilizing a first charge current to charge the node at a first rate; and	The Data Sheet includes a section called "Driver Characteristics." That section indicates that the MC33253 generates a first current of up to 1A to charge the gate node.
after a predetermined time period, maintaining the voltage on the node at the gate supervoltage utilizing a second charge current, less than the first charge current, to charge the MOS power transistor gate to the gate supervoltage at a at a second rate, wherein said second rate is slower than said first rate.	The Data Sheet includes a section called "Driver Characteristics." That section indicates that the MC33253 generates a second current of up to 100mA to charge the gate node after a predetermined period of time.

Claim 15 of U.S. Patent No. 5,359,244	
Claim Language	**Description of where each claim element is found in Motorola's MC33253**
The method of claim 14, wherein said step of charging the node connected to the gate thereof at the first rate comprises charging the node using a first and a second gate drive circuit.	As described above in connection with claim 1, the MC33253 includes a first and second gate drive circuits.

EXHIBIT C–2

Claim 1 of U.S. Patent No. 5,359,244	
Claim Language	**Description of where each claim element is found in Motorola's MC33883**
A circuit for driving a MOS power transistor, comprising:	Motorola literature found at http://e-www.motorola.com/files/analog/rich_media/webcast_slides/RMWCS_ANALOG_POWERICS.pdf indicates that the MC33883 is a "pre-driver." It drives a MOS power transistor.
a first gate drive circuit for charge pumping a node connected to a gate of the MOS power transistor to a gate supervoltage higher than a positive supply voltage by at least an amount equal to a threshold voltage of the MOS power transistor, wherein the first gate drive circuit utilizes a first charge current to charge the MOS power transistor gate to the gate supervoltage at a first rate;	Motorola data sheet, designated "Order Number: MC33883/D" (herein the "Data Sheet"), includes a Figure 1 showing the "Principal Building Blocks" of the MC33883. Figure 1 contains a block labeled "Charge Pump" that is connected to the gate of the MOS power transistor through a block labeled "Output." Within these blocks is a circuit that generates a first current of up to 1A at the output designated GATE_HS.
a second gate drive circuit for charge pumping the node connected to the gate of the MOS power transistor to maintain the voltage on such node at the gate supervoltage, wherein the second gate drive circuit utilizes a second charge current, less than the first charge current, to charge the MOS power transistor gate to the gate supervoltage at a second rate which is slower than the first rate; and	The Data Sheet includes a Figure 1 showing the "Principal Building Blocks" of the MC33883. Figure 1 contains a block labeled "Charge Pump" that is connected to the gate of the MOS power transistor through a block labeled "Output." Upon information and belief, within these blocks is a circuit that generates a second current of up to 100mA at the output designated GATE_HS.
a control circuit, wherein the control circuit enables the first and second gate drive circuits when the MOS power transistor is initially turned on, and thereafter disables the first gate drive circuit after a selected period of time.	The Data Sheet includes a Figure 1 showing the "Principal Building Blocks" of the MC33883. Figure 1 contains a block labeled "Logic" connected through other blocks to the output block. Upon information and belief, within these blocks is a control circuit.

Claim 14 of U.S. Patent No. 5,359,244	
Claim Language	**Description of where each claim element is found in Motorola's MC33883**
A method for driving a MOS power transistor, comprising the steps of:	As described above in connection with claim 1, the MC33883 drives a MOS power transistor. When the device operates, it performs a method for driving a MOS power transistor.
when the MOS power transistor is turned on, charging a node connected to a gate thereof to a gate supervoltage higher than a positive supply voltage by at least an amount equal to a threshold voltage of the MOS power transistor, utilizing a first charge current to charge the node at a first rate; and	The Data Sheet includes a section called "Device Description." That description indicates that the MC33883 generates a first current of up to 1A to charge the gate node.
after a predetermined time period, maintaining the voltage on the node at the gate supervoltage utilizing a second charge current, less than the first charge current, to charge the MOS power transistor gate to the gate supervoltage at a at a second rate, wherein said second rate is slower than said first rate.	The Data Sheet includes a section called "Device Description." That description indicates that the MC33883 generates a second current of up to 100mA to charge the gate node after a predetermined period of time.

Claim 15 of U.S. Patent No. 5,359,244	
Claim Language	**Description of where each claim element is found in Motorola's MC33883**
15. The method of claim 14, wherein said step of charging the node connected to the gate thereof at the first rate comprises charging the node using a first and a second gate drive circuit.	As described above in connection with claim 1, the MC33883 includes a first and second gate drive circuits.

Exhibit "B"

JONES DAY

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TELEPHONE: 214-220-3939 • FACSIMILE: 214-969-5100 WRITER'S DIRECT NUMBER:

832283:des
091773-012016

November 19, 2003

214/969-4556
hcgalvan@jonesday.com

VIA FACSIMILE
Bruce S. Sostek, Esq.
Thompson & Knight, LLP
1700 Pacific Avenue, Suite 3300
Dallas, Texas 75201-4693

Re: *STMicroelectronics, N.V. and STMicroelectronics, Inc. v. Motorola, Inc.*, Civil Action No. 4:03cv276

Dear Bruce:

I have reviewed the infringement contentions submitted by STMicroelectronics, Inc. Throughout its responses to Rule 3-1(a), STMicroelectronics, Inc. states that the asserted claims include "at least" the identified claim. The Patent Rules require the party claiming patent infringement to identify each claim that is allegedly infringed. STMicroelectronics, Inc. is thus precluded from asserting any additional claims at some later date.

Also, throughout its responses to Rule 3-1(f), STMicroelectronics, Inc. states that it is not presently relying on an assertion that its own "apparatus, product, device, process, method, act or instrumentality practices the claimed invention" ("Covered Product/Method"). By failing to identify any Covered Product/Method, STMicroelectronics, Inc. has waived its right to later rely on any such product or method.

Sincerely,

Hilda C. Galvan

Exhibit "C"

THOMPSON & KNIGHT LLP

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November 21, 2003

VIA FACSIMILE

Hilda C. Galvan
Jones Day
2727 North Harwood Street
Dallas, Texas 75201

Re: ***STMicroelectronics, Inc. v. Motorola, Inc.***
Civil Action No.: 4:03-CV-276

Dear Hilda:

I have reviewed your November 19, 2003 letter relating to STMicroelectronics, Inc.'s Preliminary Infringement Contentions that were served October 31, 2003. As you might expect, I do not agree with your conclusion that ST INC is "precluded from asserting any additional claims at some later date."

ST INC believes that discovery in this action, including both the documents Motorola is required to produce as part of its disclosures under Patent Rule 3–4 and our further investigation, may reveal that claims other than those identified by ST INC in its preliminary contentions are infringed by Motorola products and processes. Accordingly, consistent with Patent Rule 3–6, ST INC reserved the right to modify its infringement contentions based on information received in discovery and the claim interpretation adopted by the Court.

I note that Motorola did the same thing in its Preliminary Infringement Contentions, which states:

> Motorola reserves the right to supplement and/or amend these contentions based upon information that becomes available through discovery and as Motorola's investigation continues. Motorola reserves the right to amend its contentions following the Court's claim construction or as circumstances may warrant.

ST INC does not believe that the patent rules are to be applied inflexibly to the extent that a party's positions are deemed to be set in stone ten days after the Initial Case Management Conference. However, if that is in fact your position in this case then please be advised that Motorola has failed to identify a single accused instrumentality for 2 of its 4 patents in the Sherman action and as a result, consistent with your letter to me, Motorola will not be allowed to supplement and/or amend its contentions based upon information that may later become available through discovery or as

Motorola's investigation continues.

Please also be advised that ST will supplement or amend its infringement contentions as necessary based on the discovery process and our ongoing investigation of Motorola's infringement, or otherwise, as circumstances may warrant.

Sincerely,

Bruce S. Sostek

BSS/acs

cc: James P. Bradley

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FACSIMILE COVER LETTER

TO:	Hilda C. Galvan	FAX NO.: (214) 969-5100	PHONE NO.: (214) 220-3939
FROM:	Bruce S. Sostek		
SUBJECT:	*Motorola, Inc. v. STMicroelectronics, Inc.* *Cause No. 1:03-CV-0407*		
DATE:	November 21, 2003		
CLIENT/FILE #	071472.000002		**ATTY PHONE EXT.: 1237**
			NO. OF PAGES: 3

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Please see attached correspondence of this date.

Exhibit "D"

JONES DAY

2727 NORTH HARWOOD STREET • DALLAS, TEXAS 75201-1515

MAILING ADDRESS: P.O. BOX 660623 • DALLAS, TEXAS 75266-0623

TELEPHONE: 214-220-3939 • FACSIMILE: 214-969-5100 WRITER'S DIRECT NUMBER:

832283:des
091773-012016

November 24, 2003

214/969-4556
hcgalvan@jonesday.com

VIA FACSIMILE
Bruce S. Sostek, Esq.
Jane Politz Brandt, Esq.
Thompson & Knight, LLP
1700 Pacific Avenue, Suite 3300
Dallas, Texas 75201-4693

Re: *STMicroelectronics, N.V. and STMicroelectronics, Inc. v. Motorola, Inc.*, Civil Action No. 4:03cv276

Dear Bruce:

As set forth in my November 19th letter, Motorola's position on infringement contentions is limited to asserted claims and embodying products. As you know, by December 11, we must identify any claim terms that must be construed by the Court. In order to do so, the asserted claims must have been timely identified as required by the patent rules. The subsequent addition of asserted claims would also impact invalidity contentions and the corresponding document production. The patent rules were designed to eliminate the unnecessary delay and expense associated with untimely disclosures. Thus, we stand by our position that asserted claims are limited to those identified on October 31, 2003.

The issue of identifying asserted claims is fundamentally different from the issue of accused products. As you note, discovery may yield ***new*** information and that new information may lead to additional products being accused of infringement. We do not dispute that under those conditions preliminary infringement contentions may be supplemented, if done so in a timely manner.

Finally, based on your silence with respect to STM embodying products, there is no dispute that STM is precluded from identifying any STM embodying products.

Sincerely,

Hilda C. Galvan

cc: James Bradley, Esq.

Exhibit "E"

THOMPSON & KNIGHT LLP

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November 26, 2003

VIA FACSIMILE 214.969.5100
Hilda C. Galvan, Esq.
Jones Day
2727 North Harwood Street
Dallas, TX 75201-1515

Re: *STMicroelectronics, Inc. v. Motorola, Inc. v. STMicroelectronics, N.V., and STMicroelectronics, Inc.*
Cause No. 4:03-CV-276

Dear Hilda:

I understand that the patent rules provide for dates and deadlines for the performance of tasks in this case. Nevertheless, where you and I continue to differ on this point is the fact that I do not believe that these rules should be applied in a purely rigid and mechanistic fashion, as you propose. There are often circumstances and situations that require more flexibility or reasonable behavior, and it will remain only for Judge Davis to determine when and whether such reason and flexibility would be warranted.

As for your suggestion that you would be able to draw any definitive conclusions from the fact that I have not responded to an assertion or position contained in one of your letters, please be advised that you can and should conclude nothing from my silence, other than the fact that I have elected not to respond.

Best wishes to you for a happy and enjoyable Thanksgiving holiday.

Sincerely,

Bruce S. Sostek

BSS:psd

cc: James P. Bradley, Esq.
Mike Jones, Esq.
Clyde Siebman, Esq.

071472.000002.1672281.1

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FACSIMILE COVER LETTER

TO: Hilda C. Galvan - Phone: 214.220.3939 - Fax: 214.969.5100

FROM: Bruce S. Sostek

SUBJECT: *STMicroelectronics, Inc. v. Motorola, Inc. v. STMicroelectronics, N.V., and STMicroelectronics, Inc.*
Cause No. 4:03-CV-276

DATE: November 26, 2003

CLIENT/FILE # 071472.000002

ATTY PHONE EXT.: 1237

NO. OF PAGES: _____

PRIVILEGED & CONFIDENTIAL

Exhibit "F"

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
SHERMAN DIVISION

STMICROELECTRONICS, INC.,	§	
	§	
Plaintiff,	§	Civil Action No. 4:03-CV-276
	§	
v.	§	Judge Leonard E. Davis
	§	
MOTOROLA, INC.,	§	Jury Trial Demanded
	§	
Defendant,	§	
Counterclaim Plaintiff,	§	
	§	
v.	§	
	§	
STMICROELECTRONICS, N.V., and	§	
STMICROELECTRONICS, INC.,	§	
	§	
Counterclaim	§	
Defendants	§	

PRELIMINARY INVALIDITY CONTENTIONS

Defendant, Motorola, Inc. ("Motorola"), by and through its attorneys, hereby provides its Preliminary Invalidity Contentions pursuant to Patent Rule 3–3. Motorola's contentions are preliminary in that they reflect Motorola's knowledge and contentions at this date in the present action, and Motorola's search for prior art is ongoing. Accordingly, Motorola reserves the right to modify and supplement, without prejudice, its Preliminary Invalidity Contentions in the event that additional prior art is identified during the course of discovery.

In addition, Motorola disagrees with STMicroelectronics, Inc.'s ("STM's") interpretation of the meaning of many claim terms in the asserted claims. Motorola's contentions are based on either STM's infringement contentions set forth in its October 31, 2003 Disclosure of Asserted Claims and Preliminary Infringement Contentions, claim construction positions taken by or against STM during enforcement of this patent, and/or claim construction positions that may be

12/18/03

proposed by Motorola. Motorola's invalidity contentions do not represent Motorola's agreement or view as to the meaning of any claim term contained therein. Motorola anticipates a claim construction by the Court that will significantly affect the scope of the asserted claims, whereupon Motorola reserves the right to supplement, without prejudice, its Preliminary Invalidity Contentions in accordance with Patent Rule 3–6.

Motorola's Preliminary Invalidity Contentions with respect to U.S. Patent No. 5,812,789 are attached hereto as Exhibit A. Motorola's Preliminary Invalidity Contentions with respect to U.S. Patent No. 5,031,092 are attached as Exhibit B. Motorola's Preliminary Invalidity Contentions with respect to U.S. Patent No. 5,359,244 are attached as Exhibit C.

Dated: December 1, 2003

Respectfully submitted,

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Attorney-in-Charge
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CERTIFICATE OF SERVICE

I hereby certify that on this 1st day of December, 2003, a true and correct copy of the above and foregoing document has been forwarded via Federal Express to the following counsel:

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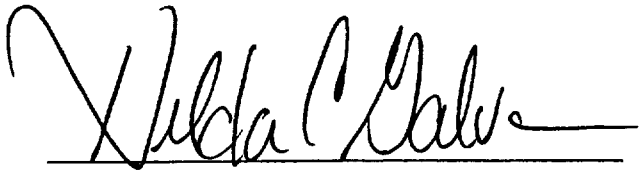

Exhibit "G"

12/19/03 (26)

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
SHERMAN DIVISION

STMICROELECTRONICS, INC., Plaintiff, vs. MOTOROLA, INC., Defendant.	CIVIL ACTION NO. 4:03–CV–276

FIRST SUPPLEMENT TO DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS OF PLAINTIFF STMICROELECTRONICS, INC.

Plaintiff STMicroelectronics, Inc. ("ST INC"), by and through its attorneys, makes this First Supplement to its Disclosure of Asserted Claims and Preliminary Infringement Contentions under Patent Rule 3–1. The asserted claims and infringement contentions, with the accompanying exhibits, are not intended to reflect, nor should they be construed to include, any other contentions.

ST INC's infringement contentions are preliminary in that they reflect ST INC's knowledge and contentions as of this date in the present action. Accordingly, ST INC reserves the right to modify and supplement, without prejudice, its Disclosure of Asserted Claims and Preliminary Infringement Contentions, including but not limited to claims asserted, products accused, and bases for the asserted infringement.

Except as modified herein, ST INC's contentions served October 31, 2003 remain applicable.

In this supplement, ST INC has amended the infringement contentions for U.S. Patent Nos. 5,812,789 and 5,031,092. The amended contentions are contained in Exhibits A and B hereto, respectively.

Respectfully submitted,

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Texas Bar No. 18855700
Attorney-in-Charge
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Max Ciccarelli
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ATTORNEYS FOR PLAINTIFF
STMICROELECTRONICS, INC.

CERTIFICATE OF SERVICE

On the 4th day of December, 2003, a copy of the foregoing was served upon the following counsel of record as indicated:

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EXHIBIT A

DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS OF PLAINTIFF STMICROELECTRONICS, INC. FOR U.S. PATENT NO. 5,812,789

ST INC makes the following infringement contentions with respect to U.S. Patent No. 5,812,789 (the "'789 patent"):

3–1(a) Each claim of each patent in suit that is allegedly infringed by each opposing party:

ST INC asserts that Motorola infringes at least Claims 1, 2, 3, 4, 5, 6, 7, 8, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, and 28.

3–1(b) Separately for each asserted claim, each accused apparatus, product, device, process, method, act or other instrumentality ("Accused Instrumentality") of each opposing party of which the party is aware. This identification shall be as specific as possible. Each product, device, and apparatus must be identified by name or model number, if known. Each method or process must be identified by name, if known, or by any product, device or apparatus which, when used, allegedly results in the practice of the claimed method or process:

ST INC asserts that Claims 1, 2, 3, 4 and 14 are infringed by the products identified below:

Motorola Products that Infringe Claims 1, 2, 3, 4 and 14
MCT4000 Transport and Video Processor
MCT4100 Transport and Video Processor
MCT5100 M-DTV Module
RD2 Reference Design Platform
Motorola's i.MX Applications Processor with Hantro's Multimedia Framework

ST INC asserts that Claims 5, 6, 7, 8, 13, 15, 16, 17, 18, 19, 20, 21, 22, 23 and 28 are infringed by the products identified below:

Motorola Products that Infringe Claims 5, 6, 7, 8, 13, 15, 16, 17, 18, 19, 20, 21, 22, 23 and 28
Motorola's i.MX Applications Processor with Hantro's Multimedia Framework

3–1(c) A chart identifying specifically where each element of each asserted claim is found within each Accused Instrumentality, including for each element that such party contends is governed by 35 U.S.C. § 112(6), the identity of the structure(s), act(s), or material(s) in the Accused Instrumentality that performs the claimed function:

The chart for each identified product is included at the identified Exhibit:

Infringing Motorola Product	Exhibit No.
MCT4000 Transport and Video Processor	A–1
MCT4100 Transport and Video Processor	A–2
MCT5100 M–DTV Module	A–3
RD2 Reference Design Platform	A–4
Motorola's i.MX Applications Processor with Hantro's Multimedia Framework	A–5

3–1(d) Whether each element of each asserted claim is claimed to be literally present or present under the doctrine of equivalents in the Accused Instrumentality:

Presently, ST INC believes that each element of each asserted claim is literally found in the accused products as described in the accompanying exhibits, but ST INC reserves the right to assert infringement under the doctrine of equivalents after further investigation and/or construction of claim terms by the Court.

3–1(e) For any patent that claims priority to an earlier application, the priority date to which each asserted claim allegedly is entitled:

The '789 patent claims a priority date of August 26, 1996.

3–1(f) If a party claiming patent infringement wishes to preserve the right to rely, for any purpose, on the assertion that its own apparatus, product, device, process, method, act, or other instrumentality practices the claimed invention, the party must identify, separately for each asserted claim, each such apparatus, product, device, process, method, act, or other instrumentality that incorporates or reflects that particular claim:

Presently, ST INC is not relying on the assertion that its own apparatus, product, device, process, method, act, or other instrumentality practices the claimed invention.

EXHIBIT A–1

Claim 1 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT4000 Transport and Video Processor**
1. An electronic system	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram;
coupled to a memory, comprising:	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram, "4MB SDRAM Video Memory";
a first device that requires access to the memory;	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram, "MPC850 Host Processor"; MCT4000 Reference Manual at page 4, paragraph 1.4.1 "-supports DMA access to/from MCT4000's External Memory";
a decoder that requires access to the memory	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Video Decoder";
sufficient to maintain real time operation; and	MCT4000 Reference Manual at page 147, paragraph 9.2.1 "real time";
a memory interface for coupling to the memory, and coupled to the first device and to the decoder,	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Memory Controller";
the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory	MCT4000 Reference Manual at page 145, paragraph 9.1 "All SDRAM accesses are controlled by the memory controller."; MCT4000 Reference Manual at page 151, paragraph 9.3.2 "The MC [Memory Controller] stores one 'on deck' request in a register which holds the address, size an client ID information. Priority among competing clients is exercised at the time of reading the data into this 'ready register'";
and a shared bus coupled to the memory the first device, and the decoder, the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram; "data" and "address & control" buses coupling the MCT4000 and the video memory.

Claim 2 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT4000 Transport and Video Processor**
2. The electronic system of claim 1, wherein: the first device is capable of having a variable bandwidth; and	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram, "MPC850 Host Processor"; On information and belief, the MPC850 Host Processor is capable of having a variable bandwidth;
the decoder is capable of having a variable bandwidth.	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Video Decoder" and at page 147, paragraph 9.2.1 "... the presence of PSI and audio data causes the video data rate to vary somewhat.".

Claim 3 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT4000 Transport and Video Processor**
3. The electronic system of claim 1, wherein the decoder comprises a video decoder.	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Video Decoder".

Claim 4 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT4000 Transport and Video Processor**
4. The electronic system of claim 1, wherein the decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard.	MCT4000 Reference Manual at page 4, paragraph 1.4.2 "... the incoming NRSS Part B compliant MPEG2 system level streams ....".

Claim 14 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT4000 Transport and Video Processor**
14. The electronic system of claim 1, wherein the fast bus comprises a memory bus.	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram; "data" and "address & control" buses coupling the MCT4000 and the video memory.

EXHIBIT A–2

Claim 1 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT4100 Transport and Video Processor**
1. An electronic system	Cadence Design Systems, Inc. *Customer Success*, Reference 804, Motorola – Entertainment Solutions Division at page 2 "...the MCT4100 with MCT4000 functionality ..." MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram;
coupled to a memory, comprising:	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram, "4MB SDRAM Video Memory";
a first device that requires access to the memory;	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram, "MPC850 Host Processor"; MCT4000 Reference Manual at page 4, paragraph 1.4.1 "-supports DMA access to/from MCT4000's External Memory";
a decoder that requires access to the memory	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Video Decoder";
sufficient to maintain real time operation; and	MCT4000 Reference Manual at page 147, paragraph 9.2.1 "real time";
a memory interface for coupling to the memory, and coupled to the first device and to the decoder,	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Memory Controller";
the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory	MCT4000 Reference Manual at page 145, paragraph 9.1 "All SDRAM accesses are controlled by the memory controller."; MCT4000 Reference Manual at page 151, paragraph 9.3.2 "The MC [Memory Controller] stores one 'on deck' request in a register which holds the address, size an client ID information. Priority among competing clients is exercised at the time of reading the data into this 'ready register'";
and a shared bus coupled to the memory the first device, and the decoder, the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram; "data" and "address & control" buses coupling the MCT4000 and the video memory.

Claim 1 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT4100 Transport and Video Processor**
simultaneously accesses the bus.	

Claim 2 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT4100 Transport and Video Processor**
2. The electronic system of claim 1, wherein: the first device is capable of having a variable bandwidth; and	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram, "MPC850 Host Processor"; On information and belief, the MPC850 Host Processor is capable of having a variable bandwidth;
the decoder is capable of having a variable bandwidth.	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Video Decoder" and at page 147, paragraph 9.2.1 "... the presence of PSI and audio data causes the video data rate to vary somewhat.".

Claim 3 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT4100 Transport and Video Processor**
3. The electronic system of claim 1, wherein the decoder comprises a video decoder.	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Video Decoder".

Claim 4 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT4100 Transport and Video Processor**
4. The electronic system of claim 1, wherein the decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard.	MCT4000 Reference Manual at page 4, paragraph 1.4.2 "... the incoming NRSS Part B compliant MPEG2 system level streams ....".

Claim 14 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's MCT4100 Transport and Video Processor
14. The electronic system of claim 1, wherein the fast bus comprises a memory bus.	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram; "data" and "address & control" buses coupling the MCT4000 and the video memory.

EXHIBIT A–3

Claim 1 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT5100 M–DTV Module**
1. An electronic system	Sampo Corporation Press Release: *Sampo Corporation Declares Motorola's M-DTV™ Module of Choice for Digital TV-Enabled Sets* at page 1 "The MCT5100 M-DTV module integrates …an MPEG decoder and controller … The MCT4000 is also included in this module …" MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram;
coupled to a memory, comprising:	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram, "4MB SDRAM Video Memory";
a first device that requires access to the memory;	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram, "MPC850 Host Processor"; MCT4000 Reference Manual at page 4, paragraph 1.4.1 "-supports DMA access to/from MCT4000's External Memory";
a decoder that requires access to the memory	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Video Decoder";
sufficient to maintain real time operation; and	MCT4000 Reference Manual at page 147, paragraph 9.2.1 "real time";
a memory interface for coupling to the memory, and coupled to the first device and to the decoder,	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Memory Controller";
the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory	MCT4000 Reference Manual at page 145, paragraph 9.1 "All SDRAM accesses are controlled by the memory controller."; MCT4000 Reference Manual at page 151, paragraph 9.3.2 "The MC [Memory Controller] stores one 'on deck' request in a register which holds the address, size an client ID information. Priority among competing clients is exercised at the time of reading the data into this 'ready register'";
and a shared bus coupled to the memory the first device, and the decoder, the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram; "data" and "address & control" buses coupling the MCT4000 and the video memory.

Claim 1 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT5100 M-DTV Module**
time when the first device simultaneously accesses the bus.	

Claim 2 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT5100 M-DTV Module**
2. The electronic system of claim 1, wherein: the first device is capable of having a variable bandwidth; and	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram, "MPC850 Host Processor"; On information and belief, the MPC850 Host Processor is capable of having a variable bandwidth;
the decoder is capable of having a variable bandwidth.	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Video Decoder" and at page 147, paragraph 9.2.1 "... the presence of PSI and audio data causes the video data rate to vary somewhat.".

Claim 3 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT5100 M-DTV Module**
3. The electronic system of claim 1, wherein the decoder comprises a video decoder.	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Video Decoder".

Claim 4 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT5100 M-DTV Module**
4. The electronic system of claim 1, wherein the decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard.	MCT4000 Reference Manual at page 4, paragraph 1.4.2 "... the incoming NRSS Part B compliant MPEG2 system level streams ....".

Claim 14 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's MCT5100 M-DTV Module**
14. The electronic system of claim 1, wherein the fast bus comprises a memory bus.	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram; "data" and "address & control" buses coupling the MCT4000 and the video memory.

EXHIBIT A–4

Claim 1 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's RD2 Reference Design Platform**
1. An electronic system	January 30, 1999 Press Release *First Collaboration of Motorola and Sarnoff Culminates in Cost-Effective Semiconductor Solution Offering for the DTV Market*, at page 1 "The RD2 features Motorola's popular MCP850 PowerPC™ processor .... Also featured are Motorola's MCT4000 ..." MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram;
coupled to a memory, comprising:	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram, "4MB SDRAM Video Memory";
a first device that requires access to the memory;	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram, "MPC850 Host Processor"; MCT4000 Reference Manual at page 4, paragraph 1.4.1 "-supports DMA access to/from MCT4000's External Memory";
a decoder that requires access to the memory	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Video Decoder";
sufficient to maintain real time operation; and	MCT4000 Reference Manual at page 147, paragraph 9.2.1 "real time";
a memory interface for coupling to the memory, and coupled to the first device and to the decoder,	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Memory Controller";
the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory	MCT4000 Reference Manual at page 145, paragraph 9.1 "All SDRAM accesses are controlled by the memory controller."; MCT4000 Reference Manual at page 151, paragraph 9.3.2 "The MC [Memory Controller] stores one 'on deck' request in a register which holds the address, size an client ID information. Priority among competing clients is exercised at the time of reading the data into this 'ready register'";
and a shared bus coupled to the memory the first device, and the decoder, the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram; "data" and "address & control" buses coupling the MCT4000 and the video memory.

Claim 1 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's RD2 Reference Design Platform
time when the first device simultaneously accesses the bus.	

Claim 2 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's RD2 Reference Design Platform
2. The electronic system of claim 1, wherein: the first device is capable of having a variable bandwidth; and	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram, "MPC850 Host Processor"; On information and belief, the MPC850 Host Processor is capable of having a variable bandwidth.
the decoder is capable of having a variable bandwidth.	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Video Decoder" and at page 147, paragraph 9.2.1 "... the presence of PSI and audio data causes the video data rate to vary somewhat.".

Claim 3 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's RD2 Reference Design Platform
3. The electronic system of claim 1, wherein the decoder comprises a video decoder.	MCT4000 Reference Manual at page 3, Fig. 1-2, MCT4000 Block Diagram, "Video Decoder".

Claim 4 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's RD2 Reference Design Platform
4. The electronic system of claim 1, wherein the decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard.	MCT4000 Reference Manual at page 4, paragraph 1.4.2 "... the incoming NRSS Part B compliant MPEG2 system level streams ....".

Claim 14 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's RD2 Reference Design Platform**
14. The electronic system of claim 1, wherein the fast bus comprises a memory bus.	MCT4000 Reference Manual at page 2, Fig. 1-1, SDTV Processor Block Diagram; "data" and "address & control" buses coupling the MCT4000 and the video memory.

EXHIBIT A–5

Claim 1 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework**
1. An electronic system	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 2 "... we have now added Hantro video-codec hardware along, with the software, to our recently announced next generation i.MX21 applications processor.";
coupled to a memory, comprising:	Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "SDRAM" and at page 15 "...memory shall be accessible via the AMBA bus ...";
a first device that requires access to the memory;	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, "...Motorola pre-processing and post-processing in hardware ... processor" and sole figure, "Post Processing" and "Pre- Processing" blocks; Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "ARM micro controller CODE";
a decoder that requires access to the memory	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, sole figure, "Video Decoder" block; Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "MPEG4 Decode" block;
sufficient to maintain real time operation; and	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 2, "Designed to deliver real-time MPEG4 and H.263 video compression and decompression ..."; and at page 3, "... the i.MX21 is designed to handle the simultaneous encode and decode of CIF resolution video... to meet the demanding requirements of real-time ... video conferencing";

Claim 1 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework**
a memory interface for coupling to the memory, and coupled to the first device and to the decoder,	Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "RAM INTERFACE";
the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, sole figure, "Bus Arbitration";
and a shared bus coupled to the memory the first device, and the decoder, the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, sole figure, "AHB Bus"; Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "AHB" bus;

Claim 2 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework**
2. The electronic system of claim 1, wherein: the first device is capable of having a variable bandwidth; and	On information and belief, the "processor" is known to be capable of having a variable bandwidth;
the decoder is capable of having a variable bandwidth.	On information and belief, the "video decoder" is known to be capable of having a variable bandwidth;

Claim 3 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework**
3. The electronic system of claim 1, wherein the decoder comprises a video decoder.	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, sole figure, "Video Decoder" block;

Claim 4 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework**
4. The electronic system of claim 1, wherein the decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard.	Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "MPEG4 Decode" block; On information and belief, an MPEG-4 decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard;

Claim 5 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework**
5. The electronic system of claim 1, further comprising an encoder coupled to the memory interface.	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, sole figure, "Video Encoder" block is coupled to the AHB bus, and hence, to the "RAM INTERFACE" coupled to the AHB bus illustrated in the Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System;

Claim 6 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework**
6. The electronic system of claim 5, wherein the decoder, the encoder and the memory interface are monolithically integrated into the first device.	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 2, sole figure, "Memory Interface" and block and at page 4, sole figure, "Video Encoder" and "Video Decoder" blocks are, on information and belief, monolithically integrated;

Claim 7 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework**
7. The electronic system of claim 5, wherein the encoder is capable of producing a bitstream that complies with the H.263 standard.	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 2 "... next generation i.MX21 applications processor. Designed to deliver real-time MPEG4 and H.263 video compression and decompression ...";

Claim 8 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework**
8. The electronic system of claim 1, wherein the decoder and the memory interface are monolithically integrated into the first device.	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 2, sole figure, "Memory Interface" and block and at page 4, sole figure, "Video Decoder" block are, on information and belief, monolithically integrated;

Claim 13 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework**
13. The electronic system of claim 1, wherein the bus has a bandwidth of at least twice the bandwidth required for the decoder to operate in real time.	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, sole figure, "AHB Bus"; Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "AHB" bus; On information and belief, the AHB bus has a bandwidth at least twice the bandwidth required for the decoder to operate in real time;

Claim 14 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework
14. The electronic system of claim 1, wherein the fast bus comprises a memory bus.	Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "AHB" bus is coupled to the "RAM INTERFACE";

Claim 15 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework
15. A computer comprising:	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 2 "... we have now added Hantro video-codec hardware along, with the software, to our recently announced next generation i.MX21 applications processor.";
processing means;	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 2, sole figure, "ARM926 CPU" block;
an input device connected to the processing means;	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 2, sole figure, "Human Interface" block "Keypad I/F";
an output device connected to the processing means;	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 2, sole figure, "Human Interface" block "LCD Control Smart LCD";
a memory connected to the processing means;	Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "SDRAM" and at page 15 "...memory shall be accessible via the AMBA bus ...";
a first device that requires access to the memory;	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, "...Motorola pre-processing and post-processing in hardware ... processor" and sole figure, "Post Processing" and "Pre- Processing" blocks;

Claim 15 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework
	Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "ARM micro controller CODE";
a decoder that requires access to the memory	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, sole figure, "Video Decoder" block; Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "MPEG4 Decode" block;
sufficient to maintain real time operation; and	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 2, "Designed to deliver real-time MPEG4 and H.263 video compression and decompression ..."; and at page 3, "... the i.MX21 is designed to handle the simultaneous encode and decode of CIF resolution video... to meet the demanding requirements of real-time ... video conferencing";
a memory interface coupled to the memory, to the first device, and to the decoder,	Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "RAM INTERFACE";
the memory interface having a means for selectively providing access for the first device and the decoder to the memory	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, sole figure, "Bus Arbitration";
and a shared bus coupled to the decoder, the first device, and the memory, the shared bus having a sufficient bandwidth to enable the decoder to operate in real time while sharing access to the bus.	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, sole figure, "AHB Bus"; Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "AHB" bus;

Claim 16 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework
16. The computer of claim 15, wherein: the first device is capable of having a variable bandwidth; and	On information and belief, the "processor" is known to be capable of having a variable bandwidth;
the decoder is capable of having a variable bandwidth.	On information and belief, the "video decoder" is known to be capable of having a variable bandwidth;

Claim 17 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework
17. The computer of claim 15, wherein the decoder comprises a video decoder.	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, sole figure, "Video Decoder" block;

Claim 18 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework
18. The computer of claim 15, wherein the decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard.	Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "MPEG4 Decode" block; On information and belief, an MPEG-4 decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard;

Claim 19 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework
19. The computer of claim 15, wherein the memory interface further comprises an arbiter for selectively providing access for the first device	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, sole figure, "Bus Arbitration";

Claim 19 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework
and the decoder to the memory.	

Claim 20 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework
20. The computer of claim 15, further comprising an encoder coupled to the memory interface.	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, sole figure, "Video Encoder" block is coupled to the AHB bus, and hence, to the "RAM INTERFACE" coupled to the AHB bus illustrated in the Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System;

Claim 21 of U.S. Patent No. 5,812,789	
Claim Language	Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework
21. The computer of claim 20, wherein the decoder, the encoder and the memory interface are monolithically integrated into the first device.	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 2, sole figure, "Memory Interface" and block and at page 4, sole figure, "Video Encoder" and "Video Decoder" blocks are, on information and belief, monolithically integrated;

Claim 22 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework**
22. The computer of claim 20, wherein the encoder is capable of producing a bitstream that complies with the H.263 standard.	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 2 "... next generation i.MX21 applications processor. Designed to deliver real-time MPEG4 and H.263 video compression and decompression ...";

Claim 23 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework**
23. The computer of claim 15, wherein the decoder and the memory interface are monolithically integrated into the first device.	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 2, sole figure, "Memory Interface" and block and at page 4, sole figure, "Video Decoder" block are, on information and belief, monolithically integrated;

Claim 28 of U.S. Patent No. 5,812,789	
Claim Language	**Description of where each claim element is found in Motorola's i.MX Applications Processors with Hantro's Multimedia Framework**
28. The computer of claim 15, wherein the shared bus has at least twice the required bandwidth for the decoder to operate in real time.	Motorola's i.MX Applications Processors with Hantro's Multimedia Framework White Paper at page 4, sole figure, "AHB Bus"; Hantro MPEG4 Codec Overview at page 14, Fig. 11, Hantro MPEG4 IP Integration into AMBA System, "AHB" bus; On information and belief, the AHB bus has a bandwidth at least twice the bandwidth required for the decoder to operate in real time;

EXHIBIT B

DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS OF PLAINTIFF STMICROELECTRONICS, INC. FOR U.S. PATENT NO. 5,031,092

ST INC makes the following infringement contentions with respect to U.S. Patent No. 5,031,092 (the "'092 patent"):

3–1 (a) Each claim of each patent in suit that is allegedly infringed by each opposing party:

ST INC asserts that Motorola infringes Claims 1, 6, 10, 11, 12, 23, 24 and 25.

3–1 (b) Separately for each asserted claim, each accused apparatus, product, device, process, method, act or other instrumentality ("Accused Instrumentality") of each opposing party of which the party is aware. This identification shall be as specific as possible. Each product, device, and apparatus must be identified by name or model number, if known. Each method or process must be identified by name, if known, or by any product, device or apparatus which, when used, allegedly results in the practice of the claimed method or process:

ST INC asserts that Claims 1, 6, 10, 12, 23, and 25 are infringed by the products identified below:

Motorola Products that Infringe Claims 1, 6, 10, 12, 23, and 25
DSP56305 24–Bit Digital Signal Processor
DSP56F801/803/805/807 16–Bit Digital Signal Processors
DSP56321 24–Bit Digital Signal Processor
DSP56362 24–Bit Digital Signal Processor
MC68332 32–Bit Microcontroller
MC68336 and MC68376 32–Bit Microcontrollers
MPC555 and MPC556 RISC Microcontrollers
MPC565 and MPC566 RISC Microcontrollers
MPC7410 RISC Microprocessor
MPC7441/7445 and MPC7450/7451/7455 RISC Microprocessors

ST INC asserts that Claims 11 and 24 are infringed by the products identified below:

Motorola Products that Infringe Claims 11 and 24
DSP56F801/803/805/807 16–Bit Digital Signal Processors
MC68332 32–Bit Microcontroller
MC68336 and MC68376 32–Bit Microcontrollers
MPC7410 RISC Microprocessor

3–1(c) A chart identifying specifically where each element of each asserted claim is found within each Accused Instrumentality, including for each element that such party contends is governed by 35 U.S.C. § 112(6), the identity of the structure(s), act(s), or material(s) in the Accused Instrumentality that performs the claimed function:

The chart for each identified product is included at the identified Exhibit:

Infringing Motorola Product	Exhibit No.
DSP56305 24–Bit Digital Signal Processor	B–1
DSP56F801/803/805/807 16–Bit Digital Signal Processors	B–2
DSP56321 24–Bit Digital Signal Processor	B–3
DSP56362 24–Bit Digital Signal Processor	B–4
MC68332 32–Bit Microcontroller	B–5
MC68336 and MC68376 32–Bit Microcontrollers	B–6
MPC555 and MPC556 RISC Microcontrollers	B–7
MPC565 and MPC566 RISC Microcontrollers	B–8
MPC7410 RISC Microprocessor	B–9
MPC7441/7445 and MPC7450/7451/7455 RISC Microprocessors	B–10

3–1(d) Whether each element of each asserted claim is claimed to be literally present or present under the doctrine of equivalents in the Accused Instrumentality:

Presently, ST INC believes that each element of each asserted claim is literally found in the accused products as described in the accompanying exhibits, but ST INC reserves the right to assert infringement under the doctrine of equivalents after further investigation and/or construction of claim terms by the Court.

3–1(e) For any patent that claims priority to an earlier application, the priority date to which each asserted claim allegedly is entitled:

Claims 1, 6, 10, 11, 12, 23, 24, and 25 of the '092 patent claim a priority date of November 16, 1983.

3–1(f) If a party claiming patent infringement wishes to preserve the right to rely, for any purpose, on the assertion that its own apparatus, product, device, process, method, act, or other instrumentality practices the claimed invention, the party must identify, separately for each asserted claim, each such apparatus, product, device, process, method, act, or other instrumentality that incorporates or reflects that particular claim:

Presently, ST INC is not relying on the assertion that its own apparatus, product, device, process, method, act, or other instrumentality practices the claimed invention.

EXHIBIT B–1

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56305 24–Bit Digital Signal Processor**
1. A microcomputer comprising	DSP56305 User's Manual at page 1-3, paragraph 1.1 "This manual describes the DSP56305 24-bit Digital Signal Processor (DSP), its memory, operating modes and peripheral modules.";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "24-Bit DSP56300 Core";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "P Memory RAM 6.5K x 24";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "P Memory RAM 6.5K x 24";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "Program Address Generator";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	DSP56305 User's Manual at page 1-14, Paragraph 1.8 "Program Data Bus (PDB)"";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "Program Decoder Controller";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "Data ALU 24 x 24*56 ->56-bit MAC";
(e) a first isolation region in said substrate, said first isolation region being of the same type of material as that of said substrate and containing all of said memory cells of said high density RAM array, and	On information and belief, the "P Memory RAM 6.5K x 24" resides in a first isolation region;

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56305 24–Bit Digital Signal Processor**
(f) a second isolation region separate from said first isolation region and being of the same type of material as that of said substrate, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the, "Data ALU 24 x 24*56 ->56-bit MAC" reside in a second isolation region;
(g) isolation means formed in said substrate for isolating said first and second regions, whereby said high density RAM is located on the same chip as said independently operation transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56305 24–Bit Digital Signal Processor**
6. A microcomputer comprising	DSP56305 User's Manual at page 1-3, paragraph 1.1 "This manual describes the DSP56305 24-bit Digital Signal Processor (DSP), its memory, operating modes and peripheral modules.";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "24-Bit DSP56300 Core";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "P Memory RAM 6.5K x 24";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "P Memory RAM 6.5K x 24";

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56305 24–Bit Digital Signal Processor
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "Program Address Generator";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	DSP56305 User's Manual at page 1-14, Paragraph 1.8 "Program Data Bus (PDB)"";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "Program Decoder Controller";
(d) a plurality of on-chip transistors comprising circuitry operably independently of the operation of said RAM,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "Data ALU 24 x 24*56 ->56-bit MAC";
(e) a first isolation well formed in said substrate of a semiconductor material of different type of material than said substrate and defining a first isolation region in said substrate, said first isolation region being of the same type of material as said substrate,	On information and belief, the "P Memory RAM 6.5K x 24" resides in a first isolation region;
(f) a second isolation well formed in said substrate of a semiconductor material of different type than said substrate, said first isolation region or said second well containing all of said memory cells of said high density RAM array, the other containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the, "Data ALU 24 x 24*56 ->56-bit MAC" reside in a second isolation region;
whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the high density RAM is protected from noise due to independent operation of the transistors.

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56305 24–Bit Digital Signal Processor**
10. A microcomputer comprising	DSP56305 User's Manual at page 1-3, paragraph 1.1 "This manual describes the DSP56305 24-bit Digital Signal Processor (DSP), its memory, operating modes and peripheral modules.";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "24-Bit DSP56300 Core";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "P Memory RAM 6.5K x 24";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "P Memory RAM 6.5K x 24";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "Program Address Generator";
(b) an instruction receiving circuit coupled to said RAM for reeving [sic] said instructions from said program stored in said RAM,	DSP56305 User's Manual at page 1-14, Paragraph 1.8 "Program Data Bus (PDB)"";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "Program Decoder Controller";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "Data ALU 24 x 24*56 ->56-bit MAC";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density RAM array, and	On information and belief, the "P Memory RAM 6.5K x 24" resides in a first isolation region;

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56305 24–Bit Digital Signal Processor**
(f) a second isolation region in said substrate separate from said firs [sic] isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the, "Data ALU 24 x 24*56 ->56-bit MAC" reside in a second isolation region;
said firs [sic] and second regions noise isolated from each other, whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 12 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56305 24–Bit Digital Signal Processor**
12. A microcomputer according to claim 10 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the DSP56305 device includes an epitaxial layer and the RAM array is located in the epitaxial layer.

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56305 24–Bit Digital Signal Processor**
23. A microcomputer comprising	DSP56305 User's Manual at page 1-3, paragraph 1.1 "This manual describes the DSP56305 24-bit Digital Signal Processor (DSP), its memory, operating modes and peripheral modules.";

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56305 24–Bit Digital Signal Processor
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "24-Bit DSP56300 Core";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "P Memory RAM 6.5K x 24";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "P Memory RAM 6.5K x 24";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "Program Address Generator";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	DSP56305 User's Manual at page 1-14, Paragraph 1.8 "Program Data Bus (PDB)"";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "Program Decoder Controller";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	DSP56305 User's Manual at page 1-14, Fig. 1-1 DSP56305 Block Diagram, "Data ALU 24 x 24*56 ->56-bit MAC";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	On information and belief, the "P Memory RAM 6.5K x 24" resides in a first isolation region;

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56305 24–Bit Digital Signal Processor
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	On information and belief, some of the transistors of the, "Data ALU 24 x 24*56 ->56-bit MAC" reside in a second isolation region;
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 25 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56305 24–Bit Digital Signal Processor
25. A microcomputer according to claim 23 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the DSP56305 device includes an epitaxial layer and the RAM array is located in the epitaxial layer.

EXHIBIT B–2

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16–Bit Digital Signal Processors
1. A microcomputer comprising	DSP56F801/803/805/807 User's Manual; at page 1-3, paragraph 1.1 "Combined on a single chip are the processing power of a DSP and the functionality of a micro controller and a flexible set of peripherals."
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56F801/803/805/807 User's Manual; at page 1-19. Fig. 1-6 "DSP 16-Bit Core";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	DSP56F801/803/805/807 User's Manual; at page 1-15, Table 1-2 "Program RAM" 1K x 16 (DSP56F801), 512 x 16 (DSP56F803), 512 x 16 (DSP56F805), 2K x 16 (DSP56F807);
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56F801/803/805/807 User's Manual; at page 1-15, Table 1-2 "Program RAM" 1K x 16 (DSP56F801), 512 x 16 (DSP56F803), 512 x 16 (DSP56F805), 2K x 16 (DSP56F807) and page 1-18 Fig. 1-5 "Program Memory";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	DSP56F801/803/805/807 User's Manual at page 1-18, Fig. 1-5 "Program Controller [PC]";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	DSP56F801/803/805/807 User's Manual at page 1-23, Table 1-3 ""PDB Program Data Bus 16-bit bi-directional, instruction word fetches";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56F801/803/805/807 User's Manual at page 1-18, Fig. 1-5 "Instr. Decoder";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	DSP56F801/803/805/807 User's Manual at page 1-18, Fig. 1-5 "Data ALU" and Motorola DSP56F803 Die Images [Substrate Level, @ ~1200x];

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16-Bit Digital Signal Processors**
(e) a first isolation region in said substrate, said first isolation region being of the same type of material as that of said substrate and containing all of said memory cells of said high density RAM array, and	Motorola DSP56F803 Die Images [Substrate Level, @ ~35x], [Substrate Level @ ~200x] and [Substrate Level @ ~1200x];
(f) a second isolation region separate from said first isolation region and being of the same type of material as that of said substrate, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	Motorola DSP56F803 Die Images [Substrate Level, @ ~200x] and [Substrate Level @ ~1200x];
(g) isolation means formed in said substrate for isolating said first and second regions, whereby said high density RAM is located on the same chip as said independently operation transistors and is protected from noise due to independent operation of said transistors.	Motorola DSP56F803 Die Images [Substrate Level, @ ~1200x].

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16-Bit Digital Signal Processors**
6. A microcomputer comprising	DSP56F801/803/805/807 User's Manual; at page 1-3, paragraph 1.1 "Combined on a single chip are the processing power of a DSP and the functionality of a micro controller and a flexible set of peripherals."
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56F801/803/805/807 User's Manual; at page 1-19. Fig. 1-6 "DSP 16-Bit Core";

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16–Bit Digital Signal Processors
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	DSP56F801/803/805/807 User's Manual; at page 1-15, Table 1-2 "Program RAM" 1K x 16 (DSP56F801), 512 x 16 (DSP56F803), 512 x 16 (DSP56F805), 2K x 16 (DSP56F807);
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56F801/803/805/807 User's Manual; at page 1-15, Table 1-2 "Program RAM" 1K x 16 (DSP56F801), 512 x 16 (DSP56F803), 512 x 16 (DSP56F805), 2K x 16 (DSP56F807) and page 1-18 Fig. 1-5 "Program Memory";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	DSP56F801/803/805/807 User's Manual at page 1-18, Fig. 1-5 "Program Controller [PC]";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	DSP56F801/803/805/807 User's Manual at page 1-23, Table 1-3 ""PDB Program Data Bus 16-bit bi-directional, instruction word fetches";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56F801/803/805/807 User's Manual at page 1-18, Fig. 1-5 "Instr. Decoder";
(d) a plurality of on-chip transistors comprising circuitry operably independently of the operation of said RAM,	DSP56F801/803/805/807 User's Manual at page 1-18, Fig. 1-5 "Data ALU" and Motorola DSP56F803 Die Images [Substrate Level, @ ~1200x];
(e) a first isolation well formed in said substrate of a semiconductor material of different type of material than said substrate and defining a first isolation region in said substrate, said first isolation region being of the same type of material as said substrate,	Motorola DSP56F803 Die Images [Substrate Level, @ ~35x], [Substrate Level @ ~200x] and [Substrate Level @ ~1200x];

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16–Bit Digital Signal Processors**
(f) a second isolation well formed in said substrate of a semiconductor material of different type than said substrate, said first isolation region or said second well containing all of said memory cells of said high density RAM array, the other containing some of said transistors which are operable independently of said operation of said RAM,	Motorola DSP56F803 Die Images [Substrate Level, @ ~200x] and [Substrate Level @ ~1200x];
whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola DSP56F803 Die Images [Substrate Level, @ ~1200x].

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16–Bit Digital Signal Processors**
10. A microcomputer comprising	DSP56F801/803/805/807 User's Manual; at page 1-3, paragraph 1.1 "Combined on a single chip are the processing power of a DSP and the functionality of a micro controller and a flexible set of peripherals."
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56F801/803/805/807 User's Manual; at page 1-19. Fig. 1-6 "DSP 16-Bit Core";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	DSP56F801/803/805/807 User's Manual; at page 1-15, Table 1-2 "Program RAM" 1K x 16 (DSP56F801), 512 x 16 (DSP56F803), 512 x 16 (DSP56F805), 2K x 16 (DSP56F807);

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16–Bit Digital Signal Processors
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56F801/803/805/807 User's Manual; at page 1-15, Table 1-2 "Program RAM" 1K x 16 (DSP56F801), 512 x 16 (DSP56F803), 512 x 16 (DSP56F805), 2K x 16 (DSP56F807) and page 1-18 Fig. 1-5 "Program Memory";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	DSP56F801/803/805/807 User's Manual at page 1-18, Fig. 1-5 "Program Controller [PC]";
(b) an instruction receiving circuit coupled to said RAM for reeving [sic] said instructions from said program stored in said RAM,	DSP56F801/803/805/807 User's Manual at page 1-23, Table 1-3 ""PDB Program Data Bus 16-bit bi-directional, instruction word fetches";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56F801/803/805/807 User's Manual at page 1-18, Fig. 1-5 "Instr. Decoder";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	DSP56F801/803/805/807 User's Manual at page 1-18, Fig. 1-5 "Data ALU" and Motorola DSP56F803 Die Images [Substrate Level, @ ~1200x];
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density RAM array, and	Motorola DSP56F803 Die Images [Substrate Level, @ ~35x], [Substrate Level @ ~200x] and [Substrate Level @ ~1200x];
(f) a second isolation region in said substrate separate from said firs [sic] isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	Motorola DSP56F803 Die Images [Substrate Level, @ ~200x] and [Substrate Level @ ~1200x];

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16-Bit Digital Signal Processors**
said firs [sic] and second regions noise isolated from each other, whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola DSP56F803 Die Images [Substrate Level, @ ~1200x].

Claim 11 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16-Bit Digital Signal Processors**
11. A microcomputer according to claim 10 wherein said first isolation region comprises a plurality of isolation regions each containing a portion of said memory cells of said RAM array.	On information and belief, the DSP56F801/803/805/807 devices comprise a plurality of isolation regions.

Claim 12 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16-Bit Digital Signal Processors**
12. A microcomputer according to claim 10 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the DSP56F801/803/805/807 devices include an epitaxial layer and the memory cells are located in the epitaxial layer.

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16–Bit Digital Signal Processors
23. A microcomputer comprising	DSP56F801/803/805/807 User's Manual; at page 1-3, paragraph 1.1 "Combined on a single chip are the processing power of a DSP and the functionality of a micro controller and a flexible set of peripherals."
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56F801/803/805/807 User's Manual; at page 1-19. Fig. 1-6 "DSP 16-Bit Core";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	DSP56F801/803/805/807 User's Manual; at page 1-15, Table 1-2 "Program RAM" 1K x 16 (DSP56F801), 512 x 16 (DSP56F803), 512 x 16 (DSP56F805), 2K x 16 (DSP56F807);
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56F801/803/805/807 User's Manual; at page 1-15, Table 1-2 "Program RAM" 1K x 16 (DSP56F801), 512 x 16 (DSP56F803), 512 x 16 (DSP56F805), 2K x 16 (DSP56F807) and page 1-18 Fig. 1-5 "Program Memory";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	DSP56F801/803/805/807 User's Manual at page 1-18, Fig. 1-5 "Program Controller [PC]";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	DSP56F801/803/805/807 User's Manual at page 1-23, Table 1-3 ""PDB Program Data Bus 16-bit bi-directional, instruction word fetches";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56F801/803/805/807 User's Manual at page 1-18, Fig. 1-5 "Instr. Decoder";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	DSP56F801/803/805/807 User's Manual at page 1-18, Fig. 1-5 "Data ALU" and Motorola DSP56F803 Die Images [Substrate Level, @ ~1200x];
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	Motorola DSP56F803 Die Images [Substrate Level, @ ~35x], [Substrate Level @ ~200x] and [Substrate Level @ ~1200x];

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16–Bit Digital Signal Processors
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	Motorola DSP56F803 Die Images [Substrate Level, @ ~200x] and [Substrate Level @ ~1200x];
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola DSP56F803 Die Images [Substrate Level, @ ~1200x].

Claim 24 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16–Bit Digital Signal Processors
24. A microcomputer according to claim 23 wherein said first isolation region comprises a plurality of isolation regions each containing a portion of said memory cells of said memory array.	On information and belief, the DSP56F801/803/805/807 devices comprise a plurality of isolation regions.

Claim 25 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56F801, DSP56F803, DSP56F805 and DSP56F807 16–Bit Digital Signal Processors
25. A microcomputer according to claim 23 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the DSP56F801/803/805/807 devices include an epitaxial layer and the memory cells are located in the epitaxial layer.

EXHIBIT B–3

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56321 24–Bit Digital Signal Processor
1. A microcomputer comprising	DSP56321 Reference Manual 24-Bit Digital Signal Processor;
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "24-Bit DSP56300 Core";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program RAM 32K x 24 bit";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program RAM 32K x 24 bit";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program Address Generator";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "PDB" and page 1-10, paragraph 1.6 "Program data bus for carrying program data throughout the core";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program Decode Controller";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Data ALU 24 x 24*56 ->56-bit MAC";
(e) a first isolation region in said substrate, said first isolation region being of the same type of material as that of said substrate and containing all of said memory cells of said high density RAM array, and	On information and belief, the "Program RAM 32K x 24 bit" resides in a first isolation region;

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56321 24–Bit Digital Signal Processor**
(f) a second isolation region separate from said first isolation region and being of the same type of material as that of said substrate, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the "Data ALU 24 x 24*56 ->56-bit MAC" reside in a second isolation region;
(g) isolation means formed in said substrate for isolating said first and second regions, whereby said high density RAM is located on the same chip as said independently operation transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56321 24–Bit Digital Signal Processor**
6. A microcomputer comprising	DSP56321 Reference Manual 24-Bit Digital Signal Processor;
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "24-Bit DSP56300 Core";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program RAM 32K x 24 bit";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program RAM 32K x 24 bit";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program Address Generator";

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56321 24–Bit Digital Signal Processor
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "PDB" and page 1-10, paragraph 1.6 "Program data bus for carrying program data throughout the core";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program Decode Controller";
(d) a plurality of on-chip transistors comprising circuitry operably independently of the operation of said RAM,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Data ALU 24 x 24*56 ->56-bit MAC";
(e) a first isolation well formed in said substrate of a semiconductor material of different type of material than said substrate and defining a first isolation region in said substrate, said first isolation region being of the same type of material as said substrate,	On information and belief, the "Program RAM 32K x 24 bit" resides in a first isolation region;
(f) a second isolation well formed in said substrate of a semiconductor material of different type than said substrate, said first isolation region or said second well containing all of said memory cells of said high density RAM array, the other containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the "Data ALU 24 x 24*56 ->56-bit MAC" reside in a second isolation region;
whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the high density RAM is protected from noise due to the independent operation of the transistors.

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56321 24–Bit Digital Signal Processor
10. A microcomputer comprising	DSP56321 Reference Manual 24-Bit Digital Signal Processor;
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "24-Bit DSP56300 Core";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program RAM 32K x 24 bit";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program RAM 32K x 24 bit";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program Address Generator";
(b) an instruction receiving circuit coupled to said RAM for reeving [sic] said instructions from said program stored in said RAM,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "PDB" and page 1-10, paragraph 1.6 "Program data bus for carrying program data throughout the core";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program Decode Controller";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Data ALU 24 x 24*56 ->56-bit MAC";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density RAM array, and	On information and belief, the "Program RAM 32K x 24 bit" resides in a first isolation region;
(f) a second isolation region in said substrate separate from said firs [sic] isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the "Data ALU 24 x 24*56 ->56-bit MAC" reside in a second isolation region;

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56321 24–Bit Digital Signal Processor**
said firs [sic] and second regions noise isolated from each other, whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 12 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56321 24–Bit Digital Signal Processor**
12. A microcomputer according to claim 10 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the DSP56321 device includes an epitaxial layer and the memory cells are located in the epitaxial layer.

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56321 24–Bit Digital Signal Processor**
23. A microcomputer comprising	DSP56321 Reference Manual 24-Bit Digital Signal Processor;
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "24-Bit DSP56300 Core";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program RAM 32K x 24 bit";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program RAM 32K x 24 bit";

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56321 24-Bit Digital Signal Processor**
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program Address Generator";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "PDB" and page 1-10, paragraph 1.6 "Program data bus for carrying program data throughout the core";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Program Decode Controller";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	DSP56321 Reference Manual at page 1-11, Fig. 1-1 DSP56321 Block Diagram, "Data ALU 24 x 24*56 ->56-bit MAC";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	On information and belief, the "Program RAM 32K x 24 bit" resides in a first isolation region;
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	On information and belief, some of the transistors of the "Data ALU 24 x 24*56 ->56-bit MAC" reside in a second isolation region;
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 25 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56321 24–Bit Digital Signal Processor
25. A microcomputer according to claim 23 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the DSP56321 device includes an epitaxial layer and the memory cells are located in the epitaxial layer.

EXHIBIT B–4

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56362 24–Bit Digital Signal Processor**
1. A microcomputer comprising	DSP56362 Reference Manual at page 1-1, paragraph 1.1 "This manual describes the DSP56362 24-bit digital signal processor (DSP), its memory, operating modes and peripheral modules.";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "24-bit DSP56300 Core";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program RAM Instr. Cache 3K x 24";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program RAM Instr. Cache 3K x 24";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program Address Generator";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "PDB" and page 1-7, paragraph 1.4.4 "Program Data Bus (PDB) for carrying program data throughout the core";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program Decode Controller";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Data ALU 24 x 24*56 -> 56-bit MAC ";
(e) a first isolation region in said substrate, said first isolation region being of the same type of material as that of said substrate and containing all of said memory cells of said high density RAM array, and	On information and belief, the "Program RAM Instr. Cache 3K x 24" resides in a first isolation region;

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56362 24–Bit Digital Signal Processor**
(f) a second isolation region separate from said first isolation region and being of the same type of material as that of said substrate, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the "Data ALU 24 x 24*56 ->56-bit MAC" reside in a second isolation region;
(g) isolation means formed in said substrate for isolating said first and second regions, whereby said high density RAM is located on the same chip as said independently operation transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56362 24–Bit Digital Signal Processor**
6. A microcomputer comprising	DSP56362 Reference Manual at page 1-1, paragraph 1.1 "This manual describes the DSP56362 24-bit digital signal processor (DSP), its memory, operating modes and peripheral modules.";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "24-bit DSP56300 Core";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program RAM Instr. Cache 3K x 24";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program RAM Instr. Cache 3K x 24";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program Address Generator";

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56362 24–Bit Digital Signal Processor
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "PDB" and page 1-7, paragraph 1.4.4 "Program Data Bus (PDB) for carrying program data throughout the core";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program Decode Controller";
(d) a plurality of on-chip transistors comprising circuitry operably independently of the operation of said RAM,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Data ALU 24 x 24*56 -> 56-bit MAC ";
(e) a first isolation well formed in said substrate of a semiconductor material of different type of material than said substrate and defining a first isolation region in said substrate, said first isolation region being of the same type of material as said substrate,	On information and belief, the "Program RAM Instr. Cache 3K x 24" resides in a first isolation region;
(f) a second isolation well formed in said substrate of a semiconductor material of different type than said substrate, said first isolation region or said second well containing all of said memory cells of said high density RAM array, the other containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the "Data ALU 24 x 24*56 ->56-bit MAC" reside in a second isolation region;
whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the high density RAM is protected from noise due to the independent operation of the transistors.

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56362 24–Bit Digital Signal Processor
10. A microcomputer comprising	DSP56362 Reference Manual at page 1-1, paragraph 1.1 "This manual describes the DSP56362 24-bit digital signal processor (DSP), its memory, operating modes and peripheral modules.";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "24-bit DSP56300 Core";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program RAM Instr. Cache 3K x 24";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program RAM Instr. Cache 3K x 24";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program Address Generator";
(b) an instruction receiving circuit coupled to said RAM for reeving [sic] said instructions from said program stored in said RAM,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "PDB" and page 1-7, paragraph 1.4.4 "Program Data Bus (PDB) for carrying program data throughout the core";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program Decode Controller";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Data ALU 24 x 24*56 -> 56-bit MAC ";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density RAM array, and	On information and belief, the "Program RAM Instr. Cache 3K x 24" resides in a first isolation region;

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56362 24–Bit Digital Signal Processor**
(f) a second isolation region in said substrate separate from said firs [sic] isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the "Data ALU 24 x 24*56 ->56-bit MAC" reside in a second isolation region;
said firs [sic] and second regions noise isolated from each other, whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 12 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56362 24–Bit Digital Signal Processor**
12. A microcomputer according to claim 10 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the DSP56362 device includes an epitaxial layer and the memory cells are located in the epitaxial layer.

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56362 24–Bit Digital Signal Processor**
23. A microcomputer comprising	DSP56362 Reference Manual at page 1-1, paragraph 1.1 "This manual describes the DSP56362 24-bit digital signal processor (DSP), its memory, operating modes and peripheral modules.";

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's DSP56362 24–Bit Digital Signal Processor**
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "24-bit DSP56300 Core";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program RAM Instr. Cache 3K x 24";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program RAM Instr. Cache 3K x 24";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program Address Generator";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "PDB" and page 1-7, paragraph 1.4.4 "Program Data Bus (PDB) for carrying program data throughout the core";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Program Decode Controller";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	DSP56362 Reference Manual at page 1-3, Fig. 1-1 DSP56362 Block Diagram, "Data ALU 24 x 24*56 -> 56-bit MAC ";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	On information and belief, the "Program RAM Instr. Cache 3K x 24" resides in a first isolation region;
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	On information and belief, some of the transistors of the "Data ALU 24 x 24*56 ->56-bit MAC" reside in a second isolation region;

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56362 24–Bit Digital Signal Processor
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 25 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's DSP56362 24–Bit Digital Signal Processor
25. A microcomputer according to claim 23 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the DSP56362 device includes an epitaxial layer and the memory cells are located in the epitaxial layer.

EXHIBIT B–5

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller
1. A microcomputer comprising	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "MC68332";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "TPU" and page 7-1 Section 7 "time processor unit (TPU)"; TPU Time Processor Unit Reference Manual, page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "2K TPURAM" and page 3-2, paragraph 3.1.5 "2 Kbytes of static RAM";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "2K TPURAM" and page 3-2, paragraph 3.1.5 "2 Kbytes of static RAM"; TPU Time Processor Unit Reference Manual, page 4-19, paragraph 4.2.10 "load microcode into the RAM",
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual, page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	TPU Time Processor Unit Reference Manual, page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstruction currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual, page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions.";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "CPU32"; Motorola MC68332 Die Image [Substrate Level @ ~800x].

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller**
(e) a first isolation region in said substrate, said first isolation region being of the same type of material as that of said substrate and containing all of said memory cells of said high density RAM array, and	Motorola MC68332 Die Image [Poly Level, @ ~30x], [Substrate Level @ ~50x] and [Substrate Level @ ~800x];
(f) a second isolation region separate from said first isolation region and being of the same type of material as that of said substrate, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	Motorola MC68332 Die Image [Substrate Level @ ~800x];
(g) isolation means formed in said substrate for isolating said first and second regions, whereby said high density RAM is located on the same chip as said independently operation transistors and is protected from noise due to independent operation of said transistors.	Motorola MC68332 Die Image [Substrate Level @ ~800x].

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller**
6. A microcomputer comprising	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "MC68332";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "TPU" and page 7-1 Section 7 "time processor unit (TPU)"; TPU Time Processor Unit Reference Manual, page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "2K TPURAM" and page 3-2, paragraph 3.1.5 "2 Kbytes of static RAM";

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller**
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "2K TPURAM" and page 3-2, paragraph 3.1.5 "2 Kbytes of static RAM"; TPU Time Processor Unit Reference Manual, page 4-19, paragraph 4.2.10 "load microcode into the RAM",
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual, page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	TPU Time Processor Unit Reference Manual, page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstruction currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual, page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions.";
(d) a plurality of on-chip transistors comprising circuitry operably independently of the operation of said RAM,	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "CPU32"; Motorola MC68332 Die Image [Substrate Level @ ~800x].
(e) a first isolation well formed in said substrate of a semiconductor material of different type of material than said substrate and defining a first isolation region in said substrate, said first isolation region being of the same type of material as said substrate,	Motorola MC68332 Die Image [Poly Level, @ ~30x], [Substrate Level @ ~50x] and [Substrate Level @ ~800x];

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller
(f) a second isolation well formed in said substrate of a semiconductor material of different type than said substrate, said first isolation region or said second well containing all of said memory cells of said high density RAM array, the other containing some of said transistors which are operable independently of said operation of said RAM,	Motorola MC68332 Die Image [Substrate Level @ ~800x];
whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MC68332 Die Image [Substrate Level @ ~800x].

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller
10. A microcomputer comprising	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "MC68332";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "TPU" and page 7-1 Section 7 "time processor unit (TPU)"; TPU Time Processor Unit Reference Manual, page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "2K TPURAM" and page 3-2, paragraph 3.1.5 "2 Kbytes of static RAM";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "2K TPURAM" and page 3-2, paragraph 3.1.5 "2 Kbytes of static RAM"; TPU Time Processor Unit Reference Manual, page 4-19, paragraph 4.2.10 "load microcode into the RAM",
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual, page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller
(b) an instruction receiving circuit coupled to said RAM for reeving [sic] said instructions from said program stored in said RAM,	TPU Time Processor Unit Reference Manual, page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstruction currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual, page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions.";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "CPU32"; Motorola MC68332 Die Image [Substrate Level @ ~800x].
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density RAM array, and	Motorola MC68332 Die Image [Poly Level, @ ~30x], [Substrate Level @ ~50x] and [Substrate Level @ ~800x];
(f) a second isolation region in said substrate separate from said firs [sic] isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	Motorola MC68332 Die Image [Substrate Level @ ~800x];
said firs [sic] and second regions noise isolated from each other, whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MC68332 Die Image [Substrate Level @ ~800x].

Claim 11 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller
11. A microcomputer according to claim 10 wherein said first isolation region comprises a plurality of isolation regions each containing a portion of said memory cells of said RAM array.	On information and belief, the MC68332 device comprises a plurality of isolation regions.

Claim 12 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller
12. A microcomputer according to claim 10 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the MC68332 device includes an epitaxial layer and the memory cells are located in the epitaxial layer.

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller
23. A microcomputer comprising	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "MC68332";
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "TPU" and page 7-1 Section 7 "time processor unit (TPU)"; TPU Time Processor Unit Reference Manual, page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "2K TPURAM" and page 3-2, paragraph 3.1.5 "2 Kbytes of static RAM";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "2K TPURAM" and page 3-2, paragraph 3.1.5 "2 Kbytes of static RAM"; TPU Time Processor Unit Reference Manual, page 4-19, paragraph 4.2.10 "load microcode into the RAM",
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual, page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	TPU Time Processor Unit Reference Manual, page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstruction currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual, page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions.";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	MC68332 User's Manual, page 3-3, Fig. 3-1 MC68332 Block Diagram "CPU32"; Motorola MC68332 Die Image [Substrate Level @ ~800x].
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	Motorola MC68332 Die Image [Poly Level, @ ~30x], [Substrate Level @ ~50x] and [Substrate Level @ ~800x];
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	Motorola MC68332 Die Image [Substrate Level @ ~800x];
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MC68332 Die Image [Substrate Level @ ~800x].

Claim 24 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller
24. A microcomputer according to claim 23 wherein said first isolation region comprises a plurality of isolation regions each containing a portion of said memory cells of said memory array.	On information and belief, the MC68332 device comprises a plurality of isolation regions.

Claim 25 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68332 32–Bit Microcontroller
25. A microcomputer according to claim 23 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the MC68332 device includes an epitaxial layer and the memory cells are located in the epitaxial layer.

EXHIBIT B–6

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68336 and MC68376 32–Bit Microcontrollers
1. A microcomputer comprising	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "MC68336/376";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "TPU" and page 11-1 Section 11 "time processor unit (TPU)"; TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "3.5 KBYTE TPURAM" and page 3.2 paragraph 3.1.9 "3.5 Kbytes of static RAM";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "3.5 KBYTE TPURAM"; TPU Time Processor Unit Reference Manual at page 4-19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstruction currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MC68336 and MC68376 32–Bit Microcontrollers**
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "CPU32"; Motorola MC68336 Die Image [Substrate Level, @ ~800x];
(e) a first isolation region in said substrate, said first isolation region being of the same type of material as that of said substrate and containing all of said memory cells of said high density RAM array, and	Motorola MC68336 Die Image [Poly Level, @ ~20x], [Substrate Level, @ ~70x] and [Substrate Level, @ ~800x];
(f) a second isolation region separate from said first isolation region and being of the same type of material as that of said substrate, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	Motorola MC68336 Die Image [Substrate Level, @ ~800x];
(g) isolation means formed in said substrate for isolating said first and second regions, whereby said high density RAM is located on the same chip as said independently operation transistors and is protected from noise due to independent operation of said transistors.	Motorola MC68336 Die Image [Substrate Level, @ ~800x];

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MC68336 and MC68376 32–Bit Microcontrollers**
6. A microcomputer comprising	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "MC68336/376";

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MC68336 and MC68376 32–Bit Microcontrollers**
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "TPU" and page 11-1 Section 11 "time processor unit (TPU)"; TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "3.5 KBYTE TPURAM" and page 3.2 paragraph 3.1.9 "3.5 Kbytes of static RAM";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "3.5 KBYTE TPURAM"; TPU Time Processor Unit Reference Manual at page 4-19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstruction currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."
(d) a plurality of on-chip transistors comprising circuitry operably independently of the operation of said RAM,	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "CPU32"; Motorola MC68336 Die Image [Substrate Level, @ ~800x];

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MC68336 and MC68376 32–Bit Microcontrollers**
(e) a first isolation well formed in said substrate of a semiconductor material of different type of material than said substrate and defining a first isolation region in said substrate, said first isolation region being of the same type of material as said substrate,	Motorola MC68336 Die Image [Poly Level, @ ~20x], [Substrate Level, @ ~70x] and [Substrate Level, @ ~800x];
(f) a second isolation well formed in said substrate of a semiconductor material of different type than said substrate, said first isolation region or said second well containing all of said memory cells of said high density RAM array, the other containing some of said transistors which are operable independently of said operation of said RAM,	Motorola MC68336 Die Image [Substrate Level, @ ~800x];
whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MC68336 Die Image [Substrate Level, @ ~800x];

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MC68336 and MC68376 32–Bit Microcontrollers**
10. A microcomputer comprising	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "MC68336/376";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "TPU" and page 11-1 Section 11 "time processor unit (TPU)"; TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MC68336 and MC68376 32–Bit Microcontrollers**
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "3.5 KBYTE TPURAM" and page 3.2 paragraph 3.1.9 "3.5 Kbytes of static RAM";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "3.5 KBYTE TPURAM"; TPU Time Processor Unit Reference Manual at page 4-19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said RAM for reeving [sic] said instructions from said program stored in said RAM,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstruction currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "CPU32"; Motorola MC68336 Die Image [Substrate Level, @ ~800x];
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density RAM array, and	Motorola MC68336 Die Image [Poly Level, @ ~20x], [Substrate Level, @ ~70x] and [Substrate Level, @ ~800x];

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68336 and MC68376 32–Bit Microcontrollers
(f) a second isolation region in said substrate separate from said firs [sic] isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	Motorola MC68336 Die Image [Substrate Level, @ ~800x];
said firs [sic] and second regions noise isolated from each other, whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MC68336 Die Image [Substrate Level, @ ~800x];

Claim 11 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68336 and MC68376 32–Bit Microcontrollers
11. A microcomputer according to claim 10 wherein said first isolation region comprises a plurality of isolation regions each containing a portion of said memory cells of said RAM array.	On information and belief, the MC68336/376 devices comprise a plurality of isolation regions.

Claim 12 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68336 and MC68376 32–Bit Microcontrollers
12. A microcomputer according to claim 10 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the MC68336/376 devices include an epitaxial layer and the memory cells are located in the epitaxial layer.

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68336 and MC68376 32–Bit Microcontrollers
23. A microcomputer comprising	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "MC68336/376";
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "TPU" and page 11-1 Section 11 "time processor unit (TPU)"; TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "3.5 KBYTE TPURAM" and page 3.2 paragraph 3.1.9 "3.5 Kbytes of static RAM";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "3.5 KBYTE TPURAM"; TPU Time Processor Unit Reference Manual at page 4-19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstruction currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	MC68336/376 User's Manual at page 3-4, Fig. 3-1 MC68336/376 Block Diagram "CPU32"; Motorola MC68336 Die Image [Substrate Level, @ ~800x];

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68336 and MC68376 32–Bit Microcontrollers
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	Motorola MC68336 Die Image [Poly Level, @ ~20x], [Substrate Level, @ ~70x] and [Substrate Level, @ ~800x];
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	Motorola MC68336 Die Image [Substrate Level, @ ~800x];
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MC68336 Die Image [Substrate Level, @ ~800x];

Claim 24 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68336 and MC68376 32–Bit Microcontrollers
24. A microcomputer according to claim 23 wherein said first isolation region comprises a plurality of isolation regions each containing a portion of said memory cells of said memory array.	On information and belief, the MC68336/376 devices comprise a plurality of isolation regions.

Claim 25 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MC68336 and MC68376 32-Bit Microcontrollers
25. A microcomputer according to claim 23 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the MC68336/376 devices include an epitaxial layer and the memory cells are located in the epitaxial layer.

EXHIBIT B–7

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC555 and MPC556 RISC Microcontrollers**
1. A microcomputer comprising	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "MPC555/MPC556";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "TPU3", page 1-4 paragraph 1.2.8 "Two Time Processor Units (TPU3)" and page 17-1 Section 17 "time processor unit 3 (TPU3)"; TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "DPTRAM" and page 1-4 paragraph 1.2.8 "6-Kbyte dual port TPU RAM ... for TPU microcode"; Motorola MPC555 Die Image [Poly Level, @ ~15x]
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "DPTRAM" and page 1-4 paragraph 1.2.8 "6-Kbyte dual port TPU RAM ... for TPU microcode"; TPU Time Processor Unit Reference Manual at page 4-19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstructions currently being executed.";

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC555 and MPC556 RISC Microcontrollers
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "192 Kbytes Flash"; Motorola MPC555 Die Image [Substrate Level @ ~800x];
(e) a first isolation region in said substrate, said first isolation region being of the same type of material as that of said substrate and containing all of said memory cells of said high density RAM array, and	Motorola MPC555 Die Image [Poly Level, @ ~15x], [Substrate Level, @ ~50x] and [Substrate Level @ ~800x];
(f) a second isolation region separate from said first isolation region and being of the same type of material as that of said substrate, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	Motorola MPC555 Die Image [Substrate Level @ ~800x];
(g) isolation means formed in said substrate for isolating said first and second regions, whereby said high density RAM is located on the same chip as said independently operation transistors and is protected from noise due to independent operation of said transistors.	Motorola MPC555 Die Image [Substrate Level @ ~800x].

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC555 and MPC556 RISC Microcontrollers
6. A microcomputer comprising	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "MPC555/MPC556";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "TPU3", page 1-4 paragraph 1.2.8 "Two Time Processor Units (TPU3)" and page 17-1 Section 17 "time processor unit 3 (TPU3)"; TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "DPTRAM" and page 1-4 paragraph 1.2.8 "6-Kbyte dual port TPU RAM ... for TPU microcode"; Motorola MPC555 Die Image [Poly Level, @ ~15x]
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "DPTRAM" and page 1-4 paragraph 1.2.8 "6-Kbyte dual port TPU RAM ... for TPU microcode"; TPU Time Processor Unit Reference Manual at page 4-19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstructions currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC555 and MPC556 RISC Microcontrollers**
(d) a plurality of on-chip transistors comprising circuitry operably independently of the operation of said RAM,	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "192 Kbytes Flash"; Motorola MPC555 Die Image [Substrate Level @ ~800x];
(e) a first isolation well formed in said substrate of a semiconductor material of different type of material than said substrate and defining a first isolation region in said substrate, said first isolation region being of the same type of material as said substrate,	Motorola MPC555 Die Image [Poly Level, @ ~15x], [Substrate Level, @ ~50x] and [Substrate Level @ ~800x];
(f) a second isolation well formed in said substrate of a semiconductor material of different type than said substrate, said first isolation region or said second well containing all of said memory cells of said high density RAM array, the other containing some of said transistors which are operable independently of said operation of said RAM,	Motorola MPC555 Die Image [Substrate Level @ ~800x];
whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MPC555 Die Image [Substrate Level @ ~800x].

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC555 and MPC556 RISC Microcontrollers**
10. A microcomputer comprising	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "MPC555/MPC556";

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC555 and MPC556 RISC Microcontrollers**
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "TPU3", page 1-4 paragraph 1.2.8 "Two Time Processor Units (TPU3)" and page 17-1 Section 17 "time processor unit 3 (TPU3)"; TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "DPTRAM" and page 1-4 paragraph 1.2.8 "6-Kbyte dual port TPU RAM ... for TPU microcode"; Motorola MPC555 Die Image [Poly Level, @ ~15x]
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "DPTRAM" and page 1-4 paragraph 1.2.8 "6-Kbyte dual port TPU RAM ... for TPU microcode"; TPU Time Processor Unit Reference Manual at page 4-19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said RAM for reeving [sic] said instructions from said program stored in said RAM,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstructions currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC555 and MPC556 RISC Microcontrollers**
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "192 Kbytes Flash"; Motorola MPC555 Die Image [Substrate Level @ ~800x];
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density RAM array, and	Motorola MPC555 Die Image [Poly Level, @ ~15x], [Substrate Level, @ ~50x] and [Substrate Level @ ~800x];
(f) a second isolation region in said substrate separate from said firs [sic] isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	Motorola MPC555 Die Image [Substrate Level @ ~800x];
said firs [sic] and second regions noise isolated from each other, whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MPC555 Die Image [Substrate Level @ ~800x].

Claim 12 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC555 and MPC556 RISC Microcontrollers**
12. A microcomputer according to claim 10 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the MPC555/MPC556 devices include an epitaxial layer and the memory cells are located in the epitaxial layer.

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC555 and MPC556 RISC Microcontrollers**
23. A microcomputer comprising	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "MPC555/MPC556";
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "TPU3", page 1-4 paragraph 1.2.8 "Two Time Processor Units (TPU3)" and page 17-1 Section 17 "time processor unit 3 (TPU3)"; TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "DPTRAM" and page 1-4 paragraph 1.2.8 "6-Kbyte dual port TPU RAM ... for TPU microcode"; Motorola MPC555 Die Image [Poly Level, @ ~15x]
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "DPTRAM" and page 1-4 paragraph 1.2.8 "6-Kbyte dual port TPU RAM ... for TPU microcode"; TPU Time Processor Unit Reference Manual at page 4-19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstructions currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC555 and MPC556 RISC Microcontrollers
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	MPC555/MPC556 User's Manual at page 1-2, Fig. 1-1 MPC555/MPC556 Block Diagram "192 Kbytes Flash"; Motorola MPC555 Die Image [Substrate Level @ ~800x];
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	Motorola MPC555 Die Image [Poly Level, @ ~15x], [Substrate Level, @ ~50x] and [Substrate Level @ ~800x];
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	Motorola MPC555 Die Image [Substrate Level @ ~800x];
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MPC555 Die Image [Substrate Level @ ~800x].

Claim 25 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC555 and MPC556 RISC Microcontrollers
25. A microcomputer according to claim 23 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the MPC555/MPC556 devices include an epitaxial layer and the memory cells are located in the epitaxial layer.

EXHIBIT B–8

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers**
1. A microcomputer comprising	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "MPC565/MPC566";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "TPU3" and page 18-1, Section 18 "The time processor unit 3 (TPU3), an enhanced version of the original TPU ..."; TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "4 Kbytes DPTRAM";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "4 Kbytes DPTRAM" and page 1-4 "... the 4-Kbyte dedicated to the third TPU3 for microcode"; TPU Time Processor Unit Reference Manual at page 4-19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstructions currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "PowerPC Core";
(e) a first isolation region in said substrate, said first isolation region being of the same type of material as that of said substrate and containing all of said memory cells of said high density RAM array, and	On information and belief, the "4 Kbytes DPTRAM" resides in a first isolation region;
(f) a second isolation region separate from said first isolation region and being of the same type of material as that of said substrate, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the, "PowerPC Core" reside in a second isolation region;
(g) isolation means formed in said substrate for isolating said first and second regions, whereby said high density RAM is located on the same chip as said independently operation transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers
6. A microcomputer comprising	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "MPC565/MPC566";

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers**
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "TPU3" and page 18-1, Section 18 "The time processor unit 3 (TPU3), an enhanced version of the original TPU ..."; TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "4 Kbytes DPTRAM";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "4 Kbytes DPTRAM" and page 1-4 "... the 4-Kbyte dedicated to the third TPU3 for microcode"; TPU Time Processor Unit Reference Manual at page 4-19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstructions currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."
(d) a plurality of on-chip transistors comprising circuitry operably independently of the operation of said RAM,	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "PowerPC Core";

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers
(e) a first isolation well formed in said substrate of a semiconductor material of different type of material than said substrate and defining a first isolation region in said substrate, said first isolation region being of the same type of material as said substrate,	On information and belief, the "4 Kbytes DPTRAM" resides in a first isolation region;
(f) a second isolation well formed in said substrate of a semiconductor material of different type than said substrate, said first isolation region or said second well containing all of said memory cells of said high density RAM array, the other containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the, "PowerPC Core" reside in a second isolation region;
whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the high density RAM is protected from noise due to the independent operation of the transistors.

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers
10. A microcomputer comprising	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "MPC565/MPC566";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "TPU3" and page 18-1, Section 18 "The time processor unit 3 (TPU3), an enhanced version of the original TPU ..."; TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "4 Kbytes DPTRAM";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "4 Kbytes DPTRAM" and page 1-4 "... the 4-Kbyte dedicated to the third TPU3 for microcode"; TPU Time Processor Unit Reference Manual at page 4-19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said RAM for reeving [sic] said instructions from said program stored in said RAM,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstructions currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "PowerPC Core";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density RAM array, and	On information and belief, the "4 Kbytes DPTRAM" resides in a first isolation region;
(f) a second isolation region in said substrate separate from said firs [sic] isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the, "PowerPC Core" reside in a second isolation region;

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers**
said firs [sic] and second regions noise isolated from each other, whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 12 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers**
12. A microcomputer according to claim 10 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the MPC565/MPC566 devices include an epitaxial layer and the memory cells are located in the epitaxial layer.

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers**
23. A microcomputer comprising	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "MPC565/MPC566";
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "TPU3" and page 18-1, Section 18 "The time processor unit 3 (TPU3), an enhanced version of the original TPU ..."; TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "TPU";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "4 Kbytes DPTRAM";

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "4 Kbytes DPTRAM" and page 1-4 "... the 4-Kbyte dedicated to the third TPU3 for microcode"; TPU Time Processor Unit Reference Manual at page 4-19, paragraph 4.2.10 "load microcode into the RAM";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "uPC" and page 4-14, paragraph 4.2.3 "The uPC contains the address used to access a microword ...";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	TPU Time Processor Unit Reference Manual at page 4-2, Fig. 4-1 TPU Detailed Block Diagram "Microinstruction Register" and page 4-18, paragraph 4.2.8 "The 32-bit register contains the microinstructions currently being executed.";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	TPU Time Processor Unit Reference Manual at page 4-8, paragraph 4.2 "Signals to the control points of the TPU are decoded from microinstructions."
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	MPC565/MPC566 Reference Manual at page 1-2, Fig. 1-1 MPC565/MPC566 Block Diagram "PowerPC Core";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	On information and belief, the "4 Kbytes DPTRAM" resides in a first isolation region;
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	On information and belief, some of the transistors of the, "PowerPC Core" reside in a second isolation region;

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 25 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC565 and MPC566 RISC Microcontrollers
25. A microcomputer according to claim 23 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the MPC565/MPC566 devices include an epitaxial layer and the memory cells are located in the epitaxial layer.

EXHIBIT B–9

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor**
1. A microcomputer comprising	MPC7410 RISC Microprocessor User's Manual at page 1-1, Paragraph 1.1 "MPC7410";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Branch Processing Unit" and page 6-22, paragraph 6.4.1 "Branch Processing Unit";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "32-Kbyte I Cache";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "32-Kbyte I Cache" and page 3-1, Chapter 3 "The MPC7410 microprocessor contains separate 32-Kbyte ... instruction and data caches ...";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Fetcher" and page 1-9, paragraph 1.2.2 "The sequential fetcher loads instructions from the instruction cache ...";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Instruction Queue" and page 1-10, paragraph 1.2.2.1 "The instruction queue (IQ) ... holds as many as six instructions ...";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Dispatch Unit" and page 6-6 "The decode/dispatch stage consists of the time it takes to fully decode the instruction ...";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "32-Kbyte D Cache" and page 1-2 "The MPC7410 has independent on-chip 32-Kbyte, eight-way, set associative, physically-addressed L1 (level-one) caches for instructions and data ..."; Motorola MPC7410 Die Image [Substrate Level, @ ~1200x];

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor**
(e) a first isolation region in said substrate, said first isolation region being of the same type of material as that of said substrate and containing all of said memory cells of said high density RAM array, and	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x];
(f) a second isolation region separate from said first isolation region and being of the same type of material as that of said substrate, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x];
(g) isolation means formed in said substrate for isolating said first and second regions, whereby said high density RAM is located on the same chip as said independently operation transistors and is protected from noise due to independent operation of said transistors.	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x].

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor**
6. A microcomputer comprising	MPC7410 RISC Microprocessor User's Manual at page 1-1, Paragraph 1.1 "MPC7410";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Branch Processing Unit" and page 6-22, paragraph 6.4.1 "Branch Processing Unit";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "32-Kbyte I Cache";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "32-Kbyte I Cache" and page 3-1, Chapter 3 "The MPC7410 microprocessor contains separate 32-Kbyte … instruction and data caches …";

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Fetcher" and page 1-9, paragraph 1.2.2 "The sequential fetcher loads instructions from the instruction cache ...";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Instruction Queue" and page 1-10, paragraph 1.2.2.1 "The instruction queue (IQ) ... holds as many as six instructions ...";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Dispatch Unit" and page 6-6 "The decode/dispatch stage consists of the time it takes to fully decode the instruction ...";
(d) a plurality of on-chip transistors comprising circuitry operably independently of the operation of said RAM,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "32-Kbyte D Cache" and page 1-2 "The MPC7410 has independent on-chip 32-Kbyte, eight-way, set associative, physically-addressed L1 (level-one) caches for instructions and data ..."; Motorola MPC7410 Die Image [Substrate Level, @ ~1200x];
(e) a first isolation well formed in said substrate of a semiconductor material of different type of material than said substrate and defining a first isolation region in said substrate, said first isolation region being of the same type of material as said substrate,	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x];
(f) a second isolation well formed in said substrate of a semiconductor material of different type than said substrate, said first isolation region or said second well containing all of said memory cells of said high density RAM array, the other containing some of said transistors which are operable independently of said operation of said RAM,	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x];

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor**
whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x].

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor**
10. A microcomputer comprising	MPC7410 RISC Microprocessor User's Manual at page 1-1, Paragraph 1.1 "MPC7410";
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Branch Processing Unit" and page 6-22, paragraph 6.4.1 "Branch Processing Unit";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "32-Kbyte I Cache";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "32-Kbyte I Cache" and page 3-1, Chapter 3 "The MPC7410 microprocessor contains separate 32-Kbyte ... instruction and data caches ...";
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Fetcher" and page 1-9, paragraph 1.2.2 "The sequential fetcher loads instructions from the instruction cache ...";
(b) an instruction receiving circuit coupled to said RAM for reeving [sic] said instructions from said program stored in said RAM,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Instruction Queue" and page 1-10, paragraph 1.2.2.1 "The instruction queue (IQ) ... holds as many as six instructions ...";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Dispatch Unit" and page 6-6 "The decode/dispatch stage consists of the time it takes to fully decode the instruction ...";

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor**
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "32-Kbyte D Cache" and page 1-2 "The MPC7410 has independent on-chip 32-Kbyte, eight-way, set associative, physically-addressed L1 (level-one) caches for instructions and data ..."; Motorola MPC7410 Die Image [Substrate Level, @ ~1200x];
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density RAM array, and	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x];
(f) a second isolation region in said substrate separate from said firs [sic] isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x];
said firs [sic] and second regions noise isolated from each other, whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x].

Claim 11 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor**
11. A microcomputer according to claim 10 wherein said first isolation region comprises a plurality of isolation regions each containing a portion of said memory cells of said RAM array.	On information and belief, the MPC7410 device comprises a plurality of isolation regions.

Claim 12 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor**
12. A microcomputer according to claim 10 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the MPC7410 device includes an epitaxial layer and the memory cells are located in the epitaxial layer.

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor**
23. A microcomputer comprising	MPC7410 RISC Microprocessor User's Manual at page 1-1, Paragraph 1.1 "MPC7410";
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Branch Processing Unit" and page 6-22, paragraph 6.4.1 "Branch Processing Unit";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "32-Kbyte I Cache";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "32-Kbyte I Cache" and page 3-1, Chapter 3 "The MPC7410 microprocessor contains separate 32-Kbyte ... instruction and data caches ...";
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Fetcher" and page 1-9, paragraph 1.2.2 "The sequential fetcher loads instructions from the instruction cache ...";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Instruction Queue" and page 1-10, paragraph 1.2.2.1 "The instruction queue (IQ) ... holds as many as six instructions ...";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "Dispatch Unit" and page 6-6 "The decode/dispatch stage consists of the time it takes to fully decode the instruction ...";

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor**
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	MPC7410 RISC Microprocessor User's Manual at page 1-4, Fig. 1-1 MPC7410 Microprocessor Block Diagram "32-Kbyte D Cache" and page 1-2 "The MPC7410 has independent on-chip 32-Kbyte, eight-way, set associative, physically-addressed L1 (level-one) caches for instructions and data ..."; Motorola MPC7410 Die Image [Substrate Level, @ ~1200x];
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x];
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x];
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	Motorola MPC7410 Die Image [Substrate Level, @ ~60x] and [Substrate Level, @ ~1200x].

Claim 24 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor**
24. A microcomputer according to claim 23 wherein said first isolation region comprises a plurality of isolation regions each containing a portion of said memory cells of said memory array.	On information and belief, the MPC7410 device comprises a plurality of isolation regions.

Claim 25 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC7410 RISC Microprocessor
25. A microcomputer according to claim 23 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the MPC7410 device includes an epitaxial layer and the memory cells are located in the epitaxial layer.

EXHIBIT B–10

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors**
1. A microcomputer comprising	MPC7450 RISC Microprocessor Family User's Manual at page 1-5, Paragraphs 1.1.1 through 1.1.4 "MPC7441", "MPC7450", "MPC7455" and "MPC7445" respectively;
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Branch Processing Unit" and page 1-13, paragraph 1.2.2.2 "Branch Processing Unit";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "32-Kbyte I Cache" and page 1-17, paragraph 1.2.4 "The MPC7451 implements separate L1 instruction and data caches. Each cache is 32-Kbyte ...";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "32-Kbyte I Cache" and page 1-17, paragraph 1.2.4 "The MPC7451 implements separate L1 instruction and data caches. Each cache is 32-Kbyte ..." ;
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Fetcher" and page 1-12, paragraph 1.2.2 "The sequential fetcher loads instructions from the instruction cache ...";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Instruction Queue" and page 1-12, paragraph 1.2.2 "The instruction queue (IQ) ... holds as many as 12 instructions ...";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Dispatch Unit" and page 1-53 "The decode/dispatch stage fully decodes each instruction ...";

Claim 1 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors**
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Integer Unit 1";
(e) a first isolation region in said substrate, said first isolation region being of the same type of material as that of said substrate and containing all of said memory cells of said high density RAM array, and	On information and belief, the "32-Kbyte I Cache" resides in a first isolation region;
(f) a second isolation region separate from said first isolation region and being of the same type of material as that of said substrate, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the "Integer Unit 1" reside in a second isolation region;
(g) isolation means formed in said substrate for isolating said first and second regions, whereby said high density RAM is located on the same chip as said independently operation transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	**Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors**
6. A microcomputer comprising	MPC7450 RISC Microprocessor Family User's Manual at page 1-5, Paragraphs 1.1.1 through 1.1.4 "MPC7441", "MPC7450", "MPC7455" and "MPC7445" respectively;

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Branch Processing Unit" and page 1-13, paragraph 1.2.2.2 "Branch Processing Unit";
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "32-Kbyte I Cache" and page 1-17, paragraph 1.2.4 "The MPC7451 implements separate L1 instruction and data caches. Each cache is 32-Kbyte ...";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "32-Kbyte I Cache" and page 1-17, paragraph 1.2.4 "The MPC7451 implements separate L1 instruction and data caches. Each cache is 32-Kbyte ..." ;
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Fetcher" and page 1-12, paragraph 1.2.2 "The sequential fetcher loads instructions from the instruction cache ...";
(b) an instruction receiving circuit coupled to said RAM for receiving said instructions from said program stored in said RAM,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Instruction Queue" and page 1-12, paragraph 1.2.2 "The instruction queue (IQ) ... holds as many as 12 instructions ...";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Dispatch Unit" and page 1-53 "The decode/dispatch stage fully decodes each instruction ...";
(d) a plurality of on-chip transistors comprising circuitry operably independently of the operation of said RAM,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Integer Unit 1";

Claim 6 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors
(e) a first isolation well formed in said substrate of a semiconductor material of different type of material than said substrate and defining a first isolation region in said substrate, said first isolation region being of the same type of material as said substrate,	On information and belief, the "32-Kbyte I Cache" resides in a first isolation region;
(f) a second isolation well formed in said substrate of a semiconductor material of different type than said substrate, said first isolation region or said second well containing all of said memory cells of said high density RAM array, the other containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the "Integer Unit 1" reside in a second isolation region;
whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the high density RAM is protected from noise due to the independent operation of the transistors.

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors
10. A microcomputer comprising	MPC7450 RISC Microprocessor Family User's Manual at page 1-5, Paragraphs 1.1.1 through 1.1.4 "MPC7441", "MPC7450", "MPC7455" and "MPC7445" respectively;
an on-chip processor and an on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Branch Processing Unit" and page 1-13, paragraph 1.2.2.2 "Branch Processing Unit";

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors
wherein said on-chip memory comprises a high density RAM array having at least 1K bytes	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "32-Kbyte I Cache" and page 1-17, paragraph 1.2.4 "The MPC7451 implements separate L1 instruction and data caches. Each cache is 32-Kbyte ...";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "32-Kbyte I Cache" and page 1-17, paragraph 1.2.4 "The MPC7451 implements separate L1 instruction and data caches. Each cache is 32-Kbyte ..." ;
(a) an instruction pointer circuit for addressing said RAM to obtain program instructions therefrom,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Fetcher" and page 1-12, paragraph 1.2.2 "The sequential fetcher loads instructions from the instruction cache ...";
(b) an instruction receiving circuit coupled to said RAM for reeving [sic] said instructions from said program stored in said RAM,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Instruction Queue" and page 1-12, paragraph 1.2.2 "The instruction queue (IQ) ... holds as many as 12 instructions ...";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Dispatch Unit" and page 1-53 "The decode/dispatch stage fully decodes each instruction ...";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said RAM,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Integer Unit 1";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density RAM array, and	On information and belief, the "32-Kbyte I Cache" resides in a first isolation region;

Claim 10 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors
(f) a second isolation region in said substrate separate from said firs [sic] isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said RAM,	On information and belief, some of the transistors of the "Integer Unit 1" reside in a second isolation region;
said firs [sic] and second regions noise isolated from each other, whereby said high density RAM is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 12 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors
12. A microcomputer according to claim 10 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the MPC7441/7445 and MPC7450/7451/7455 devices include an epitaxial layer and the memory cells are located in the epitaxial layer.

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors
23. A microcomputer comprising	MPC7450 RISC Microprocessor Family User's Manual at page 1-5, Paragraphs 1.1.1 through 1.1.4 "MPC7441", "MPC7450", "MPC7455" and "MPC7445" respectively;

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors
an on-chip processor and an on-chip writable memory on a single integrated circuit chip having a substrate of semiconductor material of a first type,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Branch Processing Unit" and page 1-13, paragraph 1.2.2.2 "Branch Processing Unit";
wherein said on-chip writable memory comprises a high density memory array having at least 1K bytes	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "32-Kbyte I Cache" and page 1-17, paragraph 1.2.4 "The MPC7451 implements separate L1 instruction and data caches. Each cache is 32-Kbyte ...";
for holding a sequence of instructions for execution by said on-chip processor, said microcomputer including:	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "32-Kbyte I Cache" and page 1-17, paragraph 1.2.4 "The MPC7451 implements separate L1 instruction and data caches. Each cache is 32-Kbyte ..." ;
(a) an instruction pointer circuit for addressing said memory array to obtain program instructions therefrom,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Fetcher" and page 1-12, paragraph 1.2.2 "The sequential fetcher loads instructions from the instruction cache ...";
(b) an instruction receiving circuit coupled to said memory array for receiving said instructions from said program stored in said memory array,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Instruction Queue" and page 1-12, paragraph 1.2.2 "The instruction queue (IQ) ... holds as many as 12 instructions ...";
(c) an instruction decoder circuit coupled to said instruction receiving circuit for decoding instructions received by said instruction receiving circuit,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Dispatch Unit" and page 1-53 "The decode/dispatch stage fully decodes each instruction ...";
(d) a plurality of on-chip transistors comprising circuitry operable independently of the operation of said memory array,	MPC7450 RISC Microprocessor Family User's Manual at page 1-4, Fig. 1-1 MPC7451 Microprocessor Block Diagram "Integer Unit 1";
(e) a first isolation region in said substrate, said first isolation region containing all of said memory cells of said high density memory array, and	On information and belief, the "32-Kbyte I Cache" resides in a first isolation region;

Claim 23 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors
(f) a second isolation region in said substrate separate from said first isolation region, said second isolation region containing some of said transistors which are operable independently of said operation of said memory array,	On information and belief, some of the transistors of the "Integer Unit 1" reside in a second isolation region;
said first and second regions noise isolated from each other, whereby said high density memory array is located on the same chip as said independently operating transistors and is protected from noise due to independent operation of said transistors.	On information and belief, the first and second isolation regions are noise isolated from each other.

Claim 25 of U.S. Patent No. 5,031,092	
Claim Language	Description of where each claim element is found in Motorola's MPC7451, MPC7441, MPC7450, MPC7455 and MPC7445 RISC Microprocessors
25. A microcomputer according to claim 23 wherein said substrate includes an epitaxial layer and said memory cells are located in said epitaxial layer.	On information and belief, the MPC7441/7445 and MPC7450/7451/7455 devices include an epitaxial layer and the memory cells are located in the epitaxial layer.

Exhibit "H"

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VIA FACSIMILE
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Re: *Motorola Inc. v. STMicroelectronics, N.V. and STMicroelectronics, Inc. v. Motorola, Inc.*, Civil Action No. 1:03cv0407

Dear Bruce:

I am in receipt of STMicroelectronic, Inc.'s First Supplement of Disclosure of Asserted Claims and Preliminary Infringement Contentions, dated December 4, 2003. Please let me know the basis for STMicroelectronics, Inc. amendment to these contentions.

I look forward to hearing from you.

Sincerely,

Hilda C. Galvan

cc: Jane Brandt, Esq. *(via facsimile)*
James Bradley, Esq. *(via facsimile)*